Exam 1

_____
Last Name, First Name

Instructions:

- *Turn off all **cell phones**, **beepers** and other **noise making devices**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for 33% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *Put your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **13** distinct pages. Sign your name and add the date below.*
- *For each circuit design, equations must **not** be used as replacements for circuit elements.*
- *For each mixed-logic circuit diagram, label inputs of each gate with the appropriate logic equations*
- *Truth tables and voltage tables must be in **counting** order.*
- *Label the inputs and outputs of each circuit with activation-levels.*
- *Boolean expression answers must be in **lexical order**,(i.e., /A before A, A before B, & D_3 before D_2).*
- *For K-maps, label **each** grouping with the appropriate equation.*

Good morning! Welcome!

Please read carefully.

Good luck & Go Gators!!!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

_____ _____
SIGN YOUR NAME DATE (10 July 2012)

Regrade comments below: Give page # and problem # and reason for the petition.

Page	Available	Points
2-3	18	
4	14	
5	11	
6	8	
7	10	
8	10	
9-11	18	
12-13	11	
TOTAL	100	

Exam 1

_____
Last Name, First Name

[14%] 1. Solve the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(4%) 3 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number 111_{10}.

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 2 min b) Determine the **<u>8-bit</u>** signed magnitude, 1's complement, and 2's complement representations of the decimal number -111_{10}.

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(2%) 2 min 1. d) What is $37_{10} + 111_{10}$ in **<u>8-bit</u>** 2's complement? You must use binary numbers to **<u>derive</u>** and determine the solution (not decimal). Remember that you must **show <u>all</u> work.**

$(37_{10}+111_{10})_{2\text{ 8-bit 2's comp}}$: _____

Exam 1

Last Name, First Name

(3%) 1. d) What is $37_{10} - 111_{10}$ in **8-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.**

3 min

$(37_{10} - 111_{10})_{2\ 8\text{-bit}\ 2\text{'s comp}}$: _____

(2%) e) What is $111_{10} - 37_{10}$ in **8-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.**

3 min

$(111_{10} - 37_{10})_{2\ 8\text{-bit}\ 2\text{'s comp}}$: _____

[4%] 2. Answer the following short Quartus-related questions. Show **ALL** work.

(2%) a) What is the difference between a timing simulation and a functional simulation?

2 min

(2%) b) If there are two inputs, A(L) and B(H), (written as A_L and B_H, respectively in a schematic entry [bdf] file), how does Quartus treat these signals of two different actuation levels, i.e., what are the differences on how Quartus uses them.

2 min

Exam 1

Last Name, First Name

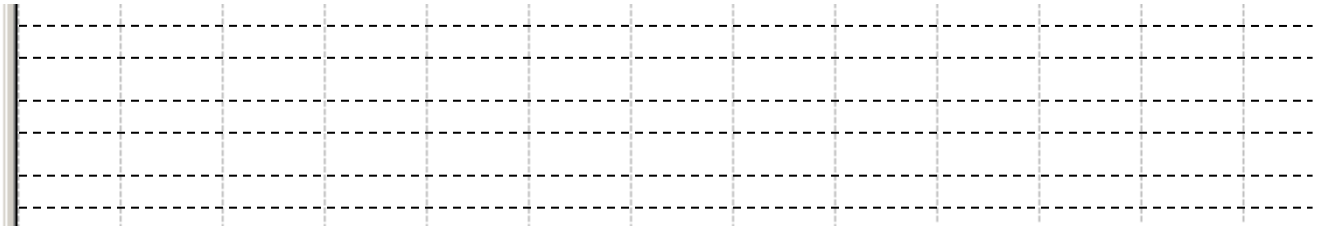
[14%] 3. Answer the following questions.

(3%) 2 min

a) Sketch the bdf file so that it looks like what you would create in Quartus for the equation Y = /(A * /B) with A(L), B(H), Y(L) using the **minimum number** of gates.

(3%) 3 min

b) Draw a **complete** timing diagram, exactly as Quartus would; include 10ns propagation delays, as Quartus would. Label the inputs and output and the time axis.

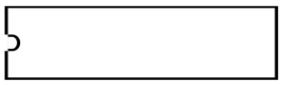


(4%) 2 min

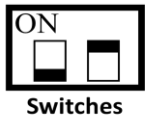
c) Draw the required switch circuits and LED circuit to complete the circuit design for this problem. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions.

(4%) 5 min

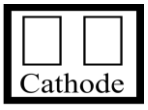
d) Draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits** for **part c** and the logic from **part a**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don't know what chip you used, so assume whatever pin numbers you want, along with the **normal** power and ground pins. Label the pin numbers **in part a**. Label the wires for each of the inputs and outputs (A, B, and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions.



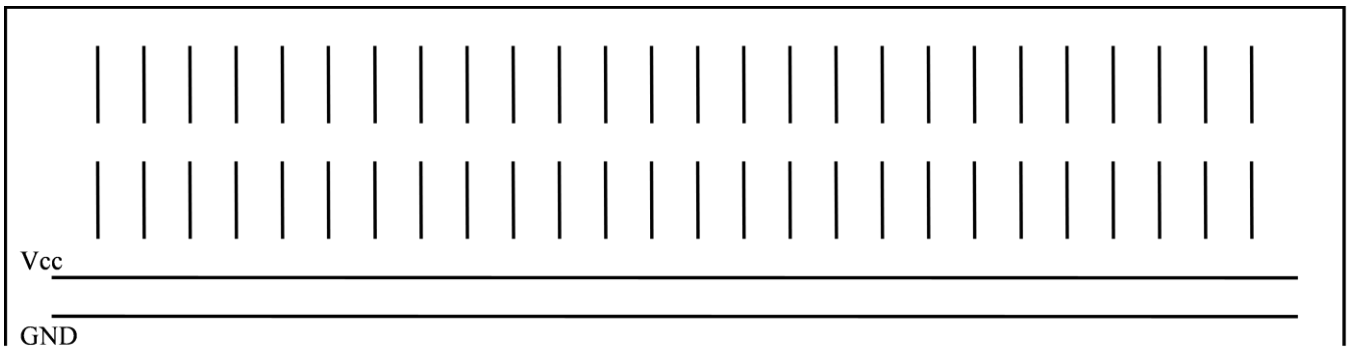
14-pin Chip



Switches



LEDs



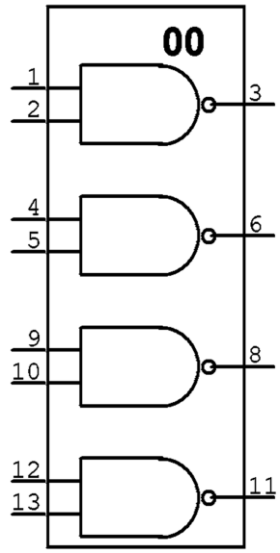
Exam 1

Last Name, First Name

[7%] 4. Directly implement the below equation with a mixed-logic circuit diagram. (Do **NOT** simplify the equation.) Use only gates of the 74HC00 (or their mixed-logic equivalents). Use the **minimum number of gates** required. Use the appropriate mixed-logic symbols. You are free to choose the activation levels. Label the pin **numbers** for your circuit design.

5 min

$$Go = \overline{\left[\left(\overline{\overline{(\bar{G} + A)} + \bar{A}\bar{T}}\right)\bar{O}\right]} + \overline{R\,\bar{S}}$$



G( )___

A( )___

T( )___

O( )___ ____Go( )

R( )___

S( )___

[4%] 5. Find the MSOP **or** MPOS equivalent of the below Boolean expression. Show **ALL** work.

5 min

$$Go = \overline{\left[\left(\overline{\overline{(\bar{G} + A)} + \bar{R}\bar{T}}\right)\bar{G}\right]} + \overline{G\,\bar{S}}$$

Go = _____

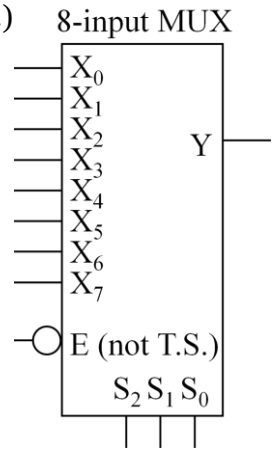
Exam 1

Last Name, First Name

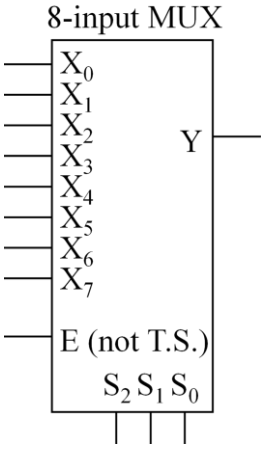
[8%] 10 min

6. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use the **minimum** number of additional SSI gates. Show all work. (The three below problems are independent.) For all of the problems, E, O and W are **active-high**. Choose efficient activation-levels for the other signals.

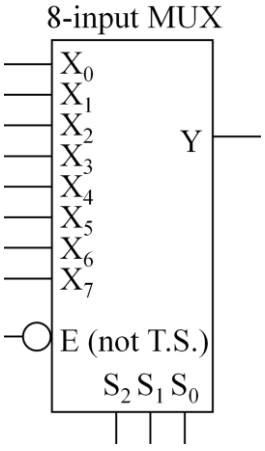
(%) a) $\mathbf{Y_0 = T*E*/B + O * /W * T}$ (Note the active-low **NON** tri-state enable.)



(%) b) $\mathbf{Y_1 = T*E*/B + O * /W * T}$ (Note the active-**HIGH** enable.)



(%) c) $\mathbf{Y_2 = /(T*E*/B + O * /W * T)}$ (Note the / at beginning of equation.)



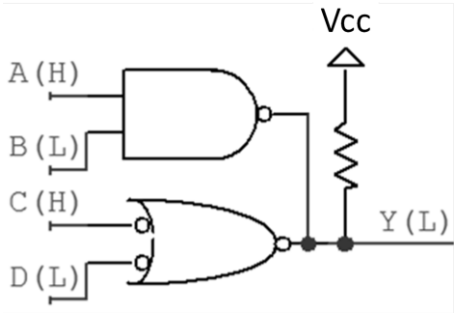
Exam 1

Last Name, First Name

10 min

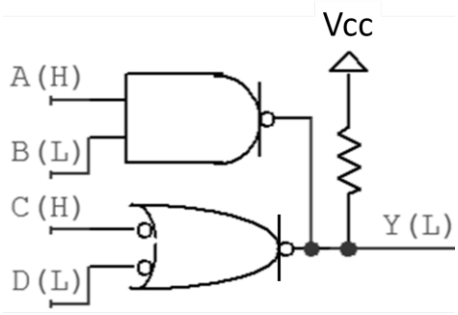
[10%] 7. Write the equations for the below circuits. Each equation should be given as a **sum-of-products** (MSOP) or a **product-of-sums** (MPOS) **Show your work!**

(%) a)



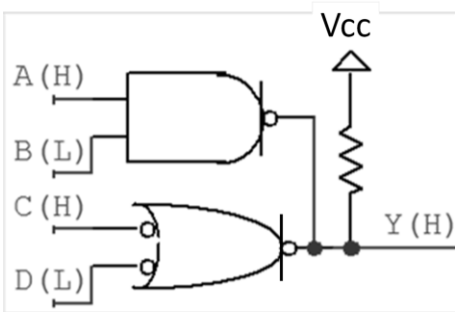
$Y_a =$ _____

(%) b)



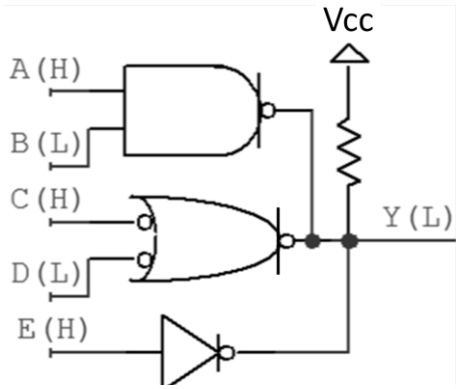
$Y_b =$ _____

(%) c)



$Y_c =$ _____

(%) d)



$Y_d =$ _____

Exam 1

Last Name, First Name

[10%] 8. Use the below equation for this problem.

$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{D} + A\bar{B}\bar{C}D + \bar{A}CD + BC\bar{D} + \bar{A}\bar{B}C\bar{D}$$

(7%) 7 min a) Simply the below equation and put the result in MSOP **and** MPOS form. Are the solutions equivalent? Explain why or why not.

CD / AB

CD / AB

Y_{MSOP} =

Y_{MPOS} =

Equivalent?:

(3%) 5 min b) If the terms ABCD=1011 and ABCD=1111, i.e., the textbook's d(11,15), are **DON'T CAREs (X)**, determine the new MSOP **and** MPOS equations. Are these solutions equivalent? Explain why or why not.

CD / AB

CD / AB

Y_{MPOS} =

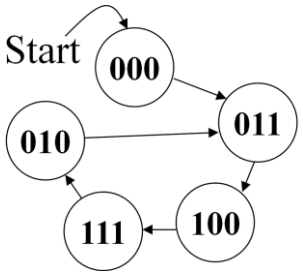
Y_{MSOP} =

Equivalent?:

Exam 1

Last Name, First Name

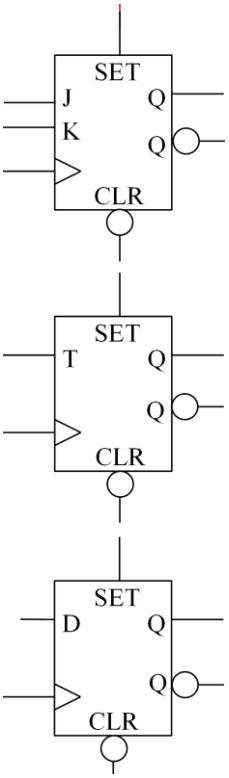
[18%] 9. Design a system that counts as shown. The system must **asynchronously** reset to the state 000 when **Start** (**active-high**) goes true. Use a JK-FF for the **most** significant bit of your design, a T-FF for the **least** significant bit, and a D-FF(s) for **any other** bits you might need. An output, **Fav** (active-low), should be true if the count is either 3 or 7. The least-significant count bit, $\mathbf{Q_0}$, should be **active-low;** all **other count bits** must be **active-high**. Note: All the given FFs have **asynchronous** clear and set inputs and are shown below.



2 min

(%) a) Draw a functional **block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your design in a box with the inputs and outputs going into or out of the box, on the left or right, respectively. This is **not** a circuit diagram.

2 min



5 min

(%) b) Complete the next-state **truth** table (**in counting order**).

Exam 1

Last Name, First Name

(%) 9. c) Find the required **simplified** (MSOP or MPOS) equations.

7 min

Exam 1

Last Name, First Name

(%) 9. d) Design the complete circuit, **minimizing** the total number of components, but using the JK-FF, T-FF, and D-FF(s) (if necessary), as described previously. All **inputs** and **outputs** of the circuit should be **clearly indicated coming into or out of** the below box. Your design must include the circuitry necessary to **asynchronous** re-start the system at "**000**" when the **Start** (active-high) signal goes true and show the active-low output **Fav** when the output is 3_{10} or 7_{10}.

5 min

Inputs

Outputs

Exam 1

Last Name, First Name

[11%] 10. In this problem you will design several multiplexers (MUX's).

(%) a) Draw a functional block diagram of a 6-input MUX with no enable. The inputs should be labeled X and S (for select lines), both with proper subscripts, if necessary. The output should be labeled Y. All signals should be active-high.

2 min

(%) b) Design **two different**, but functionally equivalent 6-input MUXs, both with **NO enable** using only 4-input and 2-input MUXs, with tri-state (T.S.) or non-tri-state (non-T.S.) enables of any activation-level. Use the two minimum cost solutions when the given MUX have the costs shown in the table. What are the costs for your two solutions? (The differences between the two designs should **not** be trivial differences.)

10 min

Item	Cost
4-input T.S. MUX	20¢
4-input non-T.S. MUX	18¢
2-input T.S. MUX	12¢
2-input non-T.S. MUX	11¢

Exam 1

Last Name, First Name

(%) 10 c) Modify one of your designs for the 6-input MUX **without** enable to make it a 6-input MUX **with** a **NON-tri-state enable**. Add as little extra cost as possible to create as low of a total cost as possible. Use **ONLY** the MUXs in the given table.

4 min

(%) d) Modify one of your designs for the 6-input MUX **without** enable to make it a 6-input MUX **with** a **tri-state enable**. Add as little extra cost as possible to create as low of a total cost as possible. Use **ONLY** the MUXs in the given table.

4 min