Instructions:
- Turn off all cell phones, beepers and other noise making devices.
- Show all work on the front of the test papers. Box each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will not be graded without an indication on the front.
- This exam counts for 33% of your total grade.
- Read each question carefully and follow the instructions.
- You may not use any notes, HW, labs, other books, or calculators.
- The point values for problems may be changed at prof's discretion.
- You must pledge and sign this page in order for a grade to be assigned.
- Put your name at the top of this test page (and, if you remove the staple, all others). Be sure your exam consists of 13 distinct pages. Sign your name and add the date below.
- For each circuit design, equations must not be used as replacements for circuit elements.
- For each mixed-logic circuit diagram, label inputs of each gate with the appropriate logic equations.
- Truth tables and voltage tables must be in counting order.
- Label the inputs and outputs of each circuit with activation-levels.
- Boolean expression answers must be in lexical order,( i.e., /A before A, A before B, & D, before D).
- For K-maps, label each grouping with the appropriate equation.

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

SIGN YOUR NAME

DATE (10 July 2012)

<table>
<thead>
<tr>
<th>Regrade comments below: Give page # and problem # and reason for the petition.</th>
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<th>Points</th>
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1. Solve the following arithmetic problems. **Remember to show ALL work here and in EVERY problem on this exam.**

   a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number $111_{10}$.

   - Binary: ______________________
   - Octal: ______________________
   - Hex: ______________________
   - BCD: ______________________

   b) Determine the **8-bit** signed magnitude, 1’s complement, and 2’s complement representations of the decimal number $-111_{10}$.

   - Signed Mag: ______________________
   - 1’s Comp: ______________________
   - 2’s Comp: ______________________

   d) What is $37_{10} + 111_{10}$ in **8-bit** 2’s complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must show all work.

   $(37_{10}+111_{10})_{2}$ 8-bit 2’s comp: ______________________
1. d) What is $37_{10} - 111_{10}$ in $8$-bit 2’s complement? You must use binary numbers to derive and determine the solution (not decimal). Remember that you must show all work.

$$(37_{10} - 111_{10})_{2\text{-bit} \text{ 2's comp}}$$

3 min

2. e) What is $111_{10} - 37_{10}$ in $8$-bit 2’s complement? You must use binary numbers to derive and determine the solution (not decimal). Remember that you must show all work.

$$(111_{10} - 37_{10})_{2\text{-bit} \text{ 2's comp}}$$

3 min

2. Answer the following short Quartus-related questions. Show ALL work.

a) What is the difference between a timing simulation and a functional simulation?

2 min

b) If there are two inputs, A(L) and B(H), (written as A_L and B_H, respectively in a schematic entry [bdf] file), how does Quartus treat these signals of two different actuation levels, i.e., what are the differences on how Quartus uses them?

2 min
3. Answer the following questions.

(3%) a) Sketch the bdf file so that it looks like what you would create in Quartus for the equation 
\[ Y = \left( \frac{A}{B} \right) \] with A(L), B(H), Y(L) using the minimum number of gates.

(3%) b) Draw a complete timing diagram, exactly as Quartus would; include 10ns propagation delays, as Quartus would. Label the inputs and output and the time axis.

(4%) c) Draw the required switch circuits and LED circuit to complete the circuit design for this problem. (These should be circuit diagrams, not layout diagrams.) Draw the switches in their true positions.

(4%) d) Draw a layout of the entire above circuit including each of the switch and LED circuits for part c and the logic from part a. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don’t know what chip you used, so assume whatever pin numbers you want, along with the normal power and ground pins. Label the pin numbers in part a. Label the wires for each of the inputs and outputs (A, B, and Y) with their activation levels. I suggest that you use labels to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch’s closure state. Draw the switches in their true positions.
4. Directly implement the below equation with a mixed-logic circuit diagram. (Do NOT simplify the equation.) Use only gates of the 74HC00 (or their mixed-logic equivalents). Use the minimum number of gates required. Use the appropriate mixed-logic symbols. You are free to choose the activation levels. Label the pin numbers for your circuit design.

\[ Go = \left[ \left( \bar{G} + A \right) + \bar{A}T \right]\bar{O} + R\bar{S} \]

G( ___ )

A( ___ )

T( ___ )

O( ___ )

R( ___ )

S( ___ )

5. Find the MSOP or MPOS equivalent of the below Boolean expression. Show ALL work.

\[ Go = \left[ \left( \bar{G} + A \right) + \bar{R}T \right]\bar{G} + \bar{G}\bar{S} \]

Go = ____________________________
6. Use the given multiplexers to design mixed-logic circuit diagrams that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use the **minimum** number of additional SSI gates. Show all work. (The three below problems are independent.) For all of the problems, E, O and W are **active-high.** Choose efficient activation-levels for the other signals.

(a) \( Y_0 = T \cdot E^* / B + O \cdot /W \cdot T \) (Note the active-low **NON** tri-state enable.)

(b) \( Y_1 = T \cdot E^* / B + O \cdot /W \cdot T \) (Note the active-**HIGH** enable.)

(c) \( Y_2 = / (T \cdot E^* / B + O \cdot /W \cdot T) \) (Note the \( / \) at beginning of equation.)
7. Write the equations for the below circuits. Each equation should be given as a sum-of-products (MSOP) or a product-of-sums (MPOS). Show your work!

(10%)

a) 
\[ Y_a = \] 

b) 
\[ Y_b = \] 

c) 
\[ Y_c = \] 

d) 
\[ Y_d = \]
8. Use the below equation for this problem.

\[ Y = \overline{A\overline{B}C\overline{D}} + A\overline{B}\overline{D} + A\overline{B}C\overline{D} + \overline{A}C\overline{D} + B\overline{C}\overline{D} + \overline{A}\overline{B}C\overline{D} \]

(a) Simply the below equation and put the result in MSOP and MPOS form. Are the solutions equivalent? Explain why or why not.

\[
\begin{array}{c}
\text{CD} \\
\text{AB}
\end{array}
\quad \quad \quad
\begin{array}{c}
\text{CD} \\
\text{AB}
\end{array}
\]

\[ Y_{\text{MSOP}} = \quad \quad \quad \quad Y_{\text{MPOS}} = \]

Equivalent?:

(b) If the terms \(ABCD=1011\) and \(ABCD=1111\), i.e., the textbook’s \(d(11,15)\), are DON’T CAREs (X), determine the new MSOP and MPOS equations. Are these solutions equivalent? Explain why or why not.

\[
\begin{array}{c}
\text{CD} \\
\text{AB}
\end{array}
\quad \quad \quad
\begin{array}{c}
\text{CD} \\
\text{AB}
\end{array}
\]

\[ Y_{\text{MPOS}} = \quad \quad \quad \quad Y_{\text{MSOP}} = \]

Equivalent?:
9. Design a system that counts as shown. The system must **asynchronously** reset to the state 000 when **Start** (active-high) goes true. Use a JK-FF for the **most** significant bit of your design, a T-FF for the **least** significant bit, and a D-FF(s) for **any other** bits you might need. An output, **Fav** (active-low), should be true if the count is either 3 or 7. The least-significant count bit, Q₀, should be active-low; all **other count bits** must be active-high. Note: All the given FFs have **asynchronous** clear and set inputs and are shown below.

(a) Draw a functional **block diagram** (showing all the inputs, all the outputs, and the functional blocks). Put your design in a box with the inputs and outputs going into or out of the box, on the left or right, respectively. This is **not** a circuit diagram.

(b) Complete the next-state **truth table** (in counting order).

<table>
<thead>
<tr>
<th>Q₀</th>
<th>Q₁</th>
<th>Q₂</th>
<th>Q₃</th>
<th>Fav</th>
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<tbody>
<tr>
<td>0</td>
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</table>
9. c) Find the required simplified (MSOP or MPOS) equations.
Design the complete circuit, **minimizing** the total number of components, but using the JK-FF, T-FF, and D-FF(s) (if necessary), as described previously. All **inputs** and **outputs** of the circuit should be clearly indicated **coming into or out of** the below box. Your design must include the circuitry necessary to **asynchronous** re-start the system at “000” when the **Start** (active-high) signal goes true and show the active-low output **Fav** when the output is $3_{10}$ or $7_{10}$.
[11%] 10. In this problem you will design several multiplexers (MUX’s).

( %) a) Draw a functional block diagram of a 6-input MUX with no enable. The inputs should be labeled X and S (for select lines), both with proper subscripts, if necessary. The output should be labeled Y. All signals should be active-high.

( %) b) Design two different, but functionally equivalent 6-input MUXs, both with NO enable using only 4-input and 2-input MUXs, with tri-state (T.S.) or non-tri-state (non-T.S.) enables of any activation-level. Use the two minimum cost solutions when the given MUX have the costs shown in the table. What are the costs for your two solutions? (The differences between the two designs should not be trivial differences.)

<table>
<thead>
<tr>
<th>Item</th>
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<tr>
<td>4-input T.S. MUX</td>
<td>20¢</td>
</tr>
<tr>
<td>4-input non-T.S. MUX</td>
<td>18¢</td>
</tr>
<tr>
<td>2-input T.S. MUX</td>
<td>12¢</td>
</tr>
<tr>
<td>2-input non-T.S. MUX</td>
<td>11¢</td>
</tr>
</tbody>
</table>
(%) 10 c) Modify one of your designs for the 6-input MUX without enable to make it a 6-input MUX with a NON-tri-state enable. Add as little extra cost as possible to create as low of a total cost as possible. Use ONLY the MUXs in the given table.

4 min

(%) 4 d) Modify one of your designs for the 6-input MUX without enable to make it a 6-input MUX with a tri-state enable. Add as little extra cost as possible to create as low of a total cost as possible. Use ONLY the MUXs in the given table.

4 min