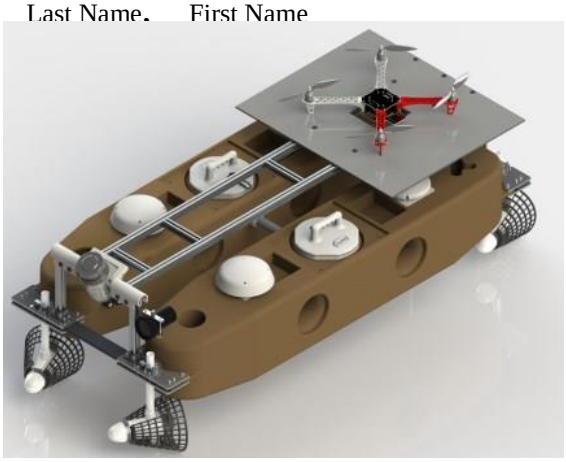
Exam 1

Last Name, First Name _____

Instructions:

Please read carefully.

- *Turn off all **cell phones** and other **noise making devices**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for 33% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *The point values for problems may be changed at prof's discretion.*



PropaGator: UF's Autonomous Surface Vehicle (Robot Boat with quadcopter)

- *You must pledge and sign this page in order for a grade to be assigned.*
- *Put your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **15** distinct pages. Sign your name and add the date below.*
- *For each circuit design, equations must **not** be used as replacements for circuit elements.*
- *For each mixed-logic circuit diagram, label inputs of each gate with the appropriate logic equations*
- *Truth tables and voltage tables must be in **counting** order.*
- *Label the inputs and outputs of each circuit with activation-levels.*
- *Boolean expression answers must be in **lexical order**,(i.e., /A before A, A before B, & D_3 before D_2).*
- *For K-maps, label **each** grouping with the appropriate equation.*

Good luck & Go Gators!!!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

_____ _____

SIGN YOUR NAME DATE (2 July 2013)

Regrade comments below: Give page # and problem # and reason for the petition.

Problem	Available	Points
1	11	
2	15	
3	6	
4	4	
5	22	
6	8	
7	10	
8	16	
9	8	
TOTAL	100	

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[11%] 1. Solve the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(4%) 4 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number 311_{10}.

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 2 min b) Determine the **<u>10-bit</u>** signed magnitude, 1's complement, and 2's complement representations of the decimal number -311_{10}.

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(2%) 3 min c) What is $128_{10} - 311_{10}$ in **<u>10-bit</u>** 2's complement? You must use binary numbers to **<u>derive</u>** and determine the solution (not decimal). Remember that you must **show <u>all</u> work.**

$(128_{10} - 311_{10})_{2\text{ 10-bit 2's comp}}$: _____

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(2%) 1. d) What is overflow? Explain and give an example.

2 min

[15%] 2. Answer the following short questions. Show **ALL** work.

(1%) a) In a Quartus simulation, what does 0 mean? What does 1 mean?

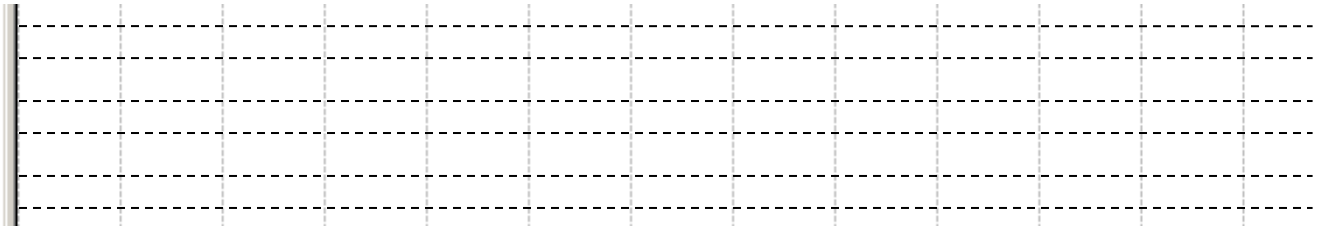
1 min

(4%) b) Draw a circuit like you would in a Quartus schematic entry [bdf] file to implement the equation Y = A*/B, where A and Y are active-low and B is active-high. Use the **minimum** number of gates.

2 min

(3%) c) Draw a **complete** timing diagram, exactly as Quartus would; include 10ns propagation delays, as Quartus would. Label the inputs and output and the time axis.

3 min



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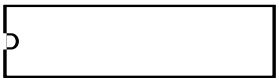
(4%) 2. d) Draw the required switch circuits and LED circuit to complete the circuit design for this problem. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions.

2 min

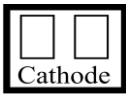
(3%) e) Draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits** for **part d** and the logic from **part b**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don't know what chip you used, so assume whatever pin numbers you want (for the 14-pin chip), along with the **normal** power and ground pins. Label the pin numbers **in part b**. Label the wires for each of the inputs and outputs (A, B, and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions.

5 min

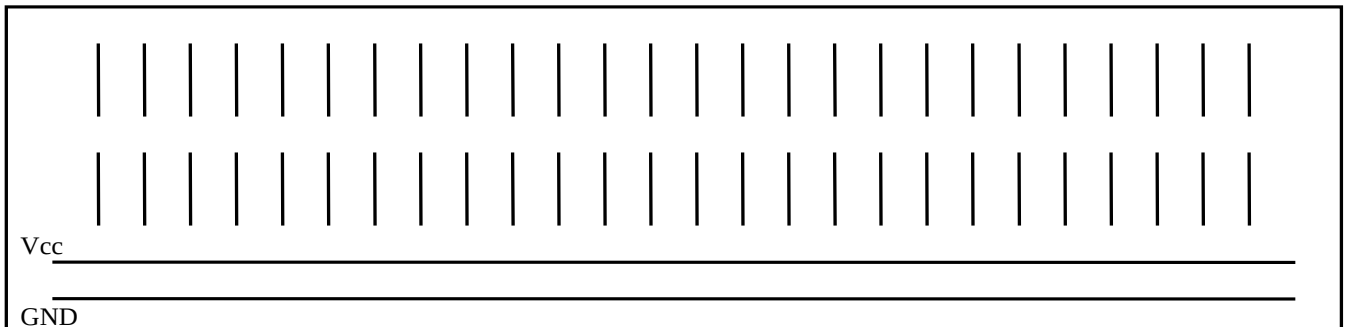


14-pin Chip

Switches



LEDs



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[6%] 5 min

3. Directly implement the below equation with a mixed-logic circuit diagram. (Do **NOT** simplify the equation.) Use only real (as specified in class) gates. Use the **minimum number of gates** required. Use the appropriate mixed-logic symbols. You are free to choose the activation levels for signals that do not already have specified activation-levels.

$$Propa = \overline{\left[\overline{\overline{(G + \overline{A})} * \overline{T}}\right] * \overline{O * R}}$$

G(L)___

A( )___

T(L)___ ___Propa(L)

O(H)___

R( )___

[4%] 5 min

4. Find the MSOP **or** MPOS equivalent of the below Boolean expression. Show **ALL** work.

$$Propa = \overline{\left[\overline{\overline{(G + \overline{A})} * \overline{T}}\right] * \overline{O * R}}$$

Propa = _____

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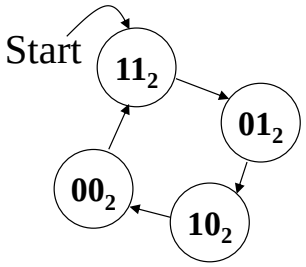
[22%] 2 min

5. Design a system that counts as shown. The system must **asynchronously** go to the state with output 11_2 when **Start** (**active-low**) goes true. Use a **T-FF** for the **most** significant bit of your design, a **JK-FF** for the **least** significant bit, and a D-FF(s) for **any other** bits you might need. An output, **Boom** (active-high), should be true if the count is 00 or 10. The least-significant count bit, $\mathbf{Q_0}$, should be **active-high;** all **other count bit(s)** must be **active-low**. Note: All the given FFs have **asynchronous** clear and set inputs as shown.

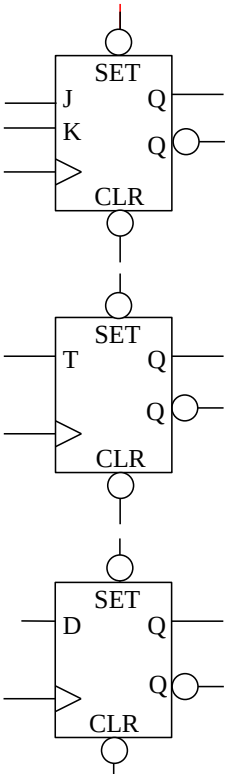


(~2%) 3 min

a) Draw a functional **block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your design in a box with the inputs and outputs going into or out of the box, on the left or right, respectively. This is **not** a circuit diagram.

Inputs

Outputs



5 min

(~4%) b) Complete the next-state **truth** table (**in counting order**).

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(~3%) 5. c) Find the required **simplified** (MSOP or MPOS) equations.

4 min

(~4%) 9. d) Design the complete circuit, **minimizing** the total number of components, but using the JK-FF, T-FF, and D-FF(s) (if necessary), as described previously. All **inputs** and **outputs** of the circuit should be **clearly indicated coming into or out of** the below box. Your design must include the circuitry necessary to **asynchronous** re-start the system at "**11**" when the **Start** (active-low) signal goes true and show the active-high output **Boom** when the output is 00 or 10.

5 min

Inputs

Outputs

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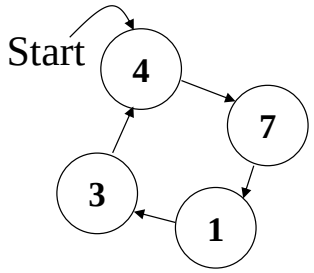
5. e) **Modify your solution** in parts a) through d) to generate the following sequence of outputs (with all bits active-high). The system must **asynchronously** reset to the state with output 4 when **Start** (**active-low**) goes true. (The rest of this is identical to part a, except that Boom should be true if the output is 1 or 3.) Repeated from part a: Use a **T-FF** for the **most** significant bit of your design, a **JK-FF** for the **least** significant bit, and a D-FF(s) for **any other** bits you might need. An output, **Boom** (active-high), should be true if the count is 00 or 10. ~~The least-significant count bit, Q_0, should be **active-high;** all **other count bit(s)** must be **active-low.**~~

2 min



(~2%) 3 min

i) Draw a functional **block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your design in a box with the inputs and outputs going into or out of the box, on the left or right, respectively. This is **not** a circuit diagram.

Inputs

Outputs

(~2%) 5 min

ii) Complete the next-state **truth** table (**in counting order**) **or** **add columns** to the

table in **part b**.

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(~2%) 3 min

5. iii) Find the required **simplified** (MSOP or MPOS) equations.

(~3%) 3 min

iv) Design the complete circuit for the problem in part e or **modify the design** in part d.

Inputs

Outputs

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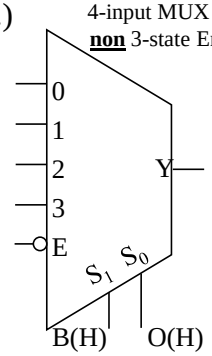
[8%] 2 min

6. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. For parts a and b, use the **minimum** number of additional SSI gates. Show all work. (The three below problems are **independent**.)

(3%) 3 min

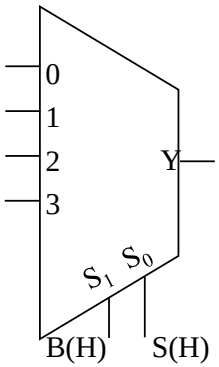
a) **UF_0 = B*/O*/T + /T*S** (Note the active-low **NON** tri-state enable.)

4-input MUX with **non** 3-state Enable



(3%) 3 min

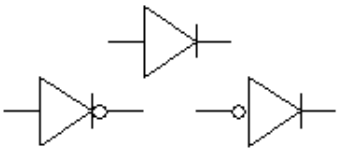
b) **UF_1 = B*/O*/T + /T*S** (Note that there is no enable.)

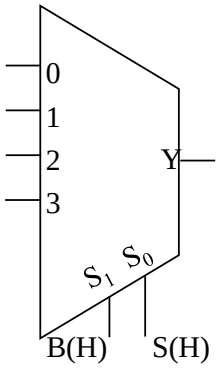


(2%) 3 min

c) Use the MUX and up to two of the **open collector** parts shown here, but **no other** components. Note that this is the same equation and MUX as in part b.

UF_2 = B*/O*/T + /T*S





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[10%] 7. Use the below equation for this problem.

$$Y = (\bar{A} + B + \bar{C}) * (\bar{A} + B + C + D) * (A + \bar{B} + C) * (A + B + \bar{C}) * (A + B + \bar{D}) * (A + B + D) * (A + \bar{C} + \bar{D})$$

(7%) a) Simply the below equation and put the result in MPOS **and** form MSOP.

7 min

CD / AB

CD / AB

Y_{MPOS} =

Y_{MSOP} =

(3%) b) If the terms ABCD=0110 and ABCD=1000, i.e., the textbook's d(6,8), are **DON'T CAREs (X)**, determine the new MPOS **and** MSOP equations. Are these solutions equivalent? Explain why or why not.

3 min

CD / AB

CD / AB

Y_{MPOS} =

Y_{MSOP} =

Equivalent?:

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[16%] 8. In this problem you will design several decoders.

(~2%) 2 min

a) Draw a truth table (with wild cards [-] or don't cares [X], if necessary) and a functional block diagram of a **1-to-2 Decoder** with **no** enable. The input(s) should be labeled X and the output(s) Y, both with proper subscripts, if necessary. All signals should be active-high.

(~2%) 2 min

b) Derive the equation(s) and design the circuit for the **1-to-2 Decoder** with **no** enable. Use only SSI (AND, NAND, OR, etc.) gates.

(~2%) 3 min

c) Draw a functional block, derive the equation(s), and design the circuit for the **1-to-2 Decoder with** an active-high enable. You **must use** the decoder from part b. Use the minimum number of additional SSI gates.

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(~2%) 3 min

8. d) Draw a truth table (with wild cards [-] or don't cares [X], if necessary) and a functional block diagram of a **2-to-4 Decoder with** an active-high enable. The input(s) should be labeled X and the output(s) Y, both with proper subscripts, if necessary. All signals should be active-high.

(~4%) 4 min

e) Design the circuit for the **2-to-4 Decoder with** an active-high enable. Use only the decoders from part b or c and use SSI gates **ONLY** if necessary.

(~4%) 4 min

8. f) Design the circuit for a **3-to-8 Decoder with** an active-high enable. Use only **2-to-4 decoders** with **3 enables**, E_0(L), E_1(H), and E_2(H), i.e., one of the enables is active-low and two enables are active-high. Use SSI gates **ONLY** if necessary.

EEL 3701—Summer 2013
Tuesday, 2 July 2013

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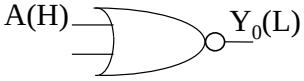
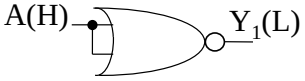
[8%] 9. What are the (SOP or POS) equations for the outputs of the following circuits?

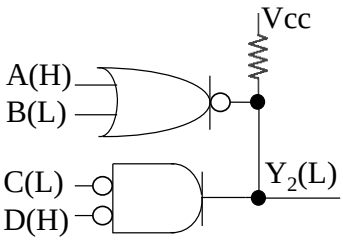
(1%) 1 min a)



(1%) 1 min b)



(3%) 3 min c)



(3%) 3 min d)