Exam 1

May the Schwartz be with you!

Last Name, First Name _____

Instructions:

- *Turn off all **cell phones** and other **noise making devices**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for 33% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators, computers, or any electronic devices.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *Boolean expression answers must be in **lexical order**, (i.e., /A before A, A before B, & D_3 before D_2).*
- *Put your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **12** distinct pages. Sign your name and add the date below.*
- *Failure to follow the below rules will result in **NO** partial credit*
  - *Truth tables, voltage tables, and timing simulations must be in **counting** order.*
  - *Label the inputs and outputs of each circuit with activation-levels.*
  - *For each mixed-logic circuit diagram, label inputs of **each** gate with the appropriate logic equations.*
  - *For K-maps, label **each** grouping with the appropriate equation.*
  - *For each circuit design, equations must **not** be used as replacements for circuit elements.*
  - *Boolean expression answers must be in **lexical order**,(i.e., /A before A, A before B, & D_3 before D_2).*

PropaGator 2: UF's Autonomous Surface Vehicle (Robot Boat with quadcopter) for RoboBoat competition

PropaGator 2 propulsion system

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

_____ _____

SIGN YOUR NAME DATE (1 July 2014)

Regrade comments below: Give page # and problem # and reason for the petition.
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Problem	Available	Points
1	11	
2	14	
3	6	
4-5	11	
6	18	
7	8	
8	12	
9-11	10	
12-14	10	
TOTAL	101	

Exam 1

Last Name, First Name

[11%] 1. Solve the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(4%) 4 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number 351_{10}.

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 2 min b) Determine the **<u>10-bit</u>** signed magnitude, 1's complement, and 2's complement representations of the decimal number -351_{10}.

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(2%) 3 min c) What is $384_{10} - 351_{10}$ in **<u>10-bit</u>** 2's complement? You must use binary numbers to **<u>derive</u>** and determine the solution (not decimal). Remember that you must **show <u>all</u> work.** (Hint: 256+128=384) Please **<u>circle</u>** your answer.

Exam 1

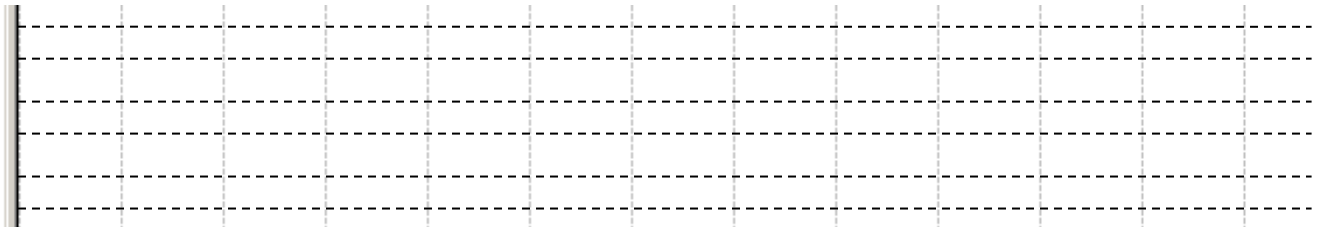
Last Name, First Name

(2%) 3 min 1. d) What is $384_{10} + 351_{10}$ in **10-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.** Please **circle** your answer.

[11%] 2. Answer the following short questions. Show **ALL** work.

(4%) 2 min a) Draw a circuit like you would in a Quartus schematic entry [bdf] file to **DIRECTLY** implement (i.e., do **NOT** simplify) the equation Y = /(A + /B), where A is active-high, and B and Y are active-low. Use the **minimum** number of gates.

(3%) 3 min b) Draw a **complete** timing diagram, exactly as Quartus would; include 10ns propagation delays, as Quartus would. Label the inputs and output and the time axis.



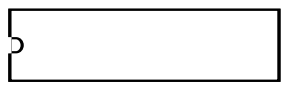
(4%) 2 min c) Draw the required switch circuits and LED circuit to complete the circuit design for this problem. The circuits should do **nothing else**. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions.

Exam 1

Last Name, First Name _____

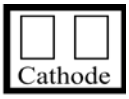
(3%) 5 min

2. d) Draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits** for **part c** and the logic from **part a**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don't know what chip you used, so assume whatever pin numbers you want (for the 14-pin chip), along with the **normal** power and ground pins. Label the pin numbers **in part a**. Label the wires for each of the inputs and outputs (A, B, and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions.

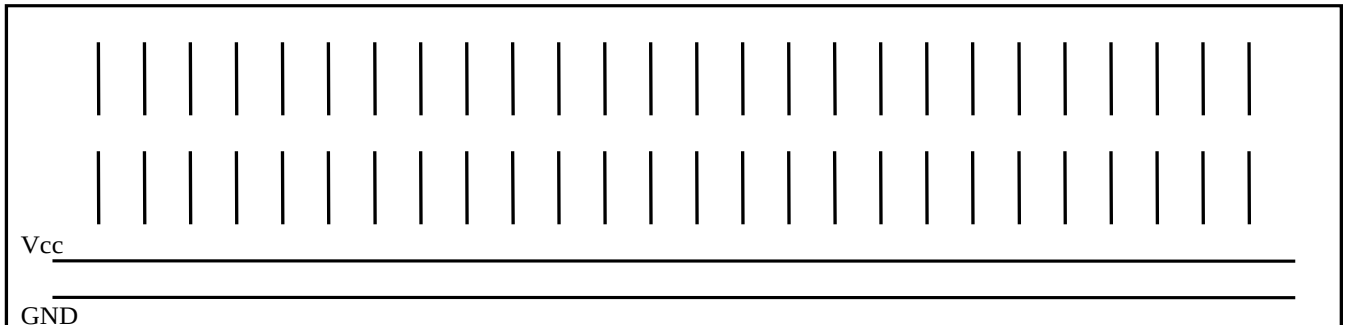


14-pin Chip

Switches

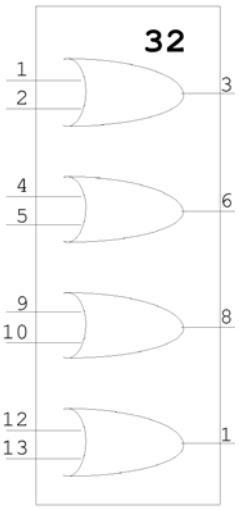


LEDs



[6%] 5 min

3. Directly implement the below equation with a mixed-logic circuit diagram. (Do **NOT** simplify the equation.) Use only gates of the 74HC32 (or their mixed-logic equivalents). **Only if necessary**, you can also use level-shifters. Use the **minimum number of gates** required. Use the appropriate mixed-logic symbols. You are free to choose the activation levels for signals that do not already have specified activation-levels.



$$Soccer = \overline{\left[\overline{(G + \bar{O})} * U\right] + \overline{S * \bar{A}}}$$

G( )___

O( )___

U(L)___ _Soccer( )

S( )___

A( )___

Exam 1

Last Name, First Name

5 min

[4%] 4. Find the MSOP **or** MPOS equivalent of the below Boolean expression. Show **ALL** work.

$$UF = \left[\overline{(G * \bar{A} * T)} + \overline{\bar{A}\bar{T}}\right] + \overline{\left(O + \overline{\bar{R}S}\right)} * O + \overline{(\bar{A} + S)}$$

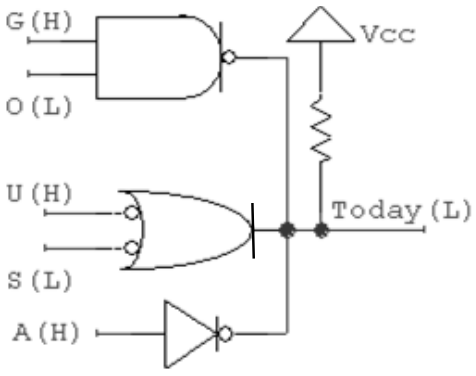
/TT

UF = _____

[7%] 5. What are the (SOP or POS) equations for the outputs of the following circuits?

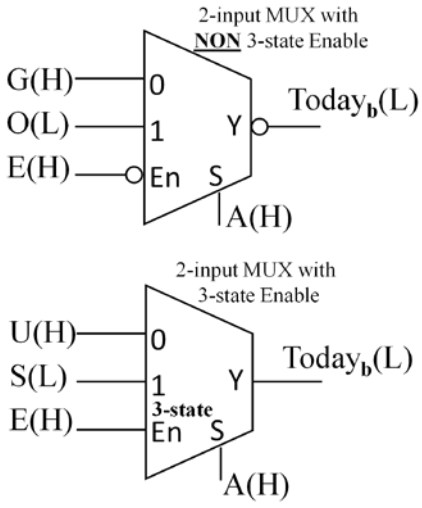
(4%) a)

4 min



(3%) b)

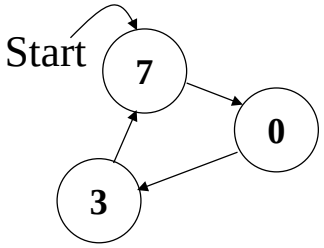
4 min



Exam 1

Last Name, First Name

[18%] 6. Design a system that "counts" as shown when E (active-low) is true; when E is false, the "count" should hold. The system must **asynchronously** go to the state "7" when **Start** (**active-high**) goes true. Use a **T-FF** for the **least** significant bit of your design, a **JK-FF** for the **most** significant bit, and a D-FF(s) for **any other** bits you might need. An output, **Zero** (active-low), should be true if the "count" is "0." The **least-significant "count" output** bit should be **active-low;** all **other "count" output** bits should be **active-high**. Note: All the given FFs have **asynchronous** clear and set inputs as shown.



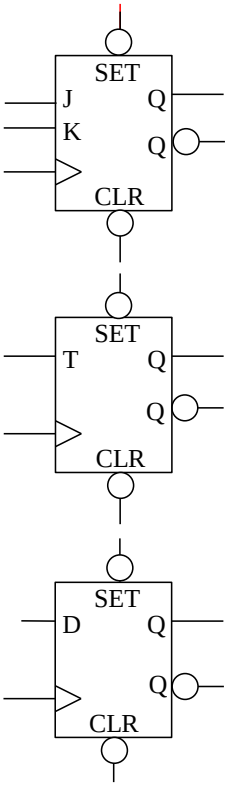
3 min

(%) a) Draw a **functional block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your design in the dashed box with the inputs and outputs going **into or out of the box**, on the left or right, respectively. This is **not** a circuit diagram.

3 min

Inputs

Outputs



5 min

(%) b) Complete the next-state **truth** table (**in counting order**).

Exam 1

Last Name, First Name

(%) 6. c) Find the required **simplified** (MSOP or MPOS) equations.

5 min

(%) d) Design the complete circuit, **minimizing** the total number of components, but using the JK-FF, T-FF, and D-FF(s) (if necessary), as described previously. All **inputs** and **outputs** of the circuit should be **clearly indicated coming into or out of** the below dashed box. Your design must include the circuitry necessary to **asynchronous** re-start the system at "**7**" when the **Start** (active-high) signal goes true and show the active-low output **Zero** when the output is "0."

5 min

Inputs

Outputs

Exam 1

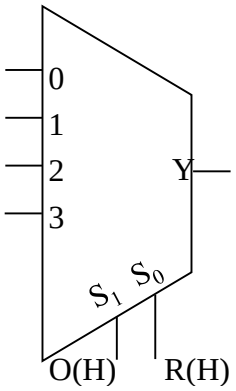
Last Name, First Name

[8%] 2 min

7. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. For parts a and b, use the **minimum** number of additional SSI gates. Show all work. (The three below problems are **independent**.)

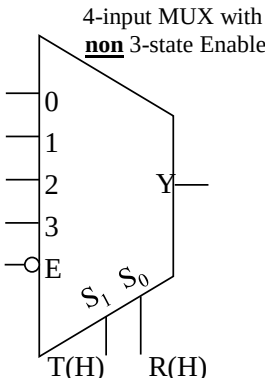
(3%) 3 min

a) **GA_0 = T*/O*R + /O*/R*S**



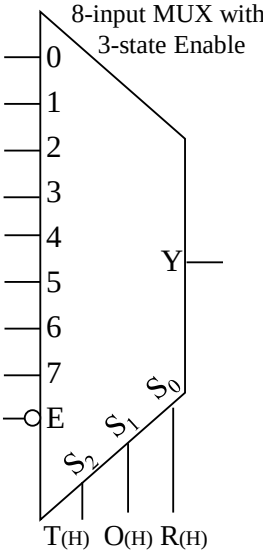
(3%) 3 min

b) **GA_1 = T*/O*R + /O*/R*S** (Note the active-low **NON** tri-state enable.)



(2%) 3 min

c) **GA_2 = T*/O*R + /O*/R*S** (Note the active-low **tri-state** enable.)



Exam 1

Last Name, First Name

[12%] 8. Use the below equation for this problem.

$$Y = \bar{A}\bar{B}CD + \bar{A}\bar{B}\bar{D} + A\bar{B}\bar{D} + AB\bar{C} + ABC\bar{D} + A\bar{C}D$$

(6%) a) Use K-maps to simply the equation and put the result in MSOP **and** form MPOS.

7 min

CD
AB

CD
AB

Y_{MSOP} =

Y_{MPOS} =

(6%) b) If the terms ABCD=0011 and ABCD=0110, i.e., the textbook's d(3,6), are **DON'T CAREs (X)**, determine the new MSOP **and** MPOS equations. Are these solutions (in part b) equivalent? Explain why or why not.

4 min

CD
AB

CD
AB

Y_{MSOP} =

Y_{MPOS} =

Equivalent?:

Exam 1

Last Name, First Name

[3%] 5 min

9. Design a **2-input** MUX with active-low **non** **tri-state enable** using only SSI (AND, NOR, etc.) gates. The enable is E(L), the output is Y(H), the input(s) and select line(s) should be number subscripted as in our class notes and labs. First draw a **functional block diagram** and then show **ALL** the work in your design process.

[4%] 5 min

10. Design a **4-input MUX** with **non** **tri-state enable** using only 2-input MUXes (from the previous problem) and the **minimum** number of SSI gates. The overall enable is E(L), the output is Y(H), the input(s) and select line(s) should be number subscripted as in our class notes and labs. First draw a **functional block diagram** and then show **ALL** the work in your design process.

Exam 1

Last Name, First Name

[3%] 11. Design a **5-input MUX** with **non tri-state enable** using **only the functional block diagrams from the last two problems**, and SSI gates, **ONLY if necessary**. The overall enable is E(L), the output is Y(H), the input(s) and select line(s) should be number subscripted as in our class notes and labs.

4 min

[~~4~~3%] 12. Design a **2-input MUX** with active-low **tri-state enable** using only the minimum number of SSI gates and a tri-state buffer, if necessary. The enable is E(L), the output is Y(H), the input(s) and select line(s) should be number subscripted as in our class notes and labs. Show **ALL** work in your design process.

4 min

Exam 1

Last Name, First Name

[4%] 5 min

13. Design a 4-input MUX with with active-low **tri-state enable** using only 2-input MUXes (from the previous problem), the minimum number of tri-state buffers, if necessary. The overall tri-state enable is E(L), the output is Y(H), the input(s) and select line(s) should be number subscripted as in our class notes and labs. First draw a **functional block diagram** and then show **ALL** the work in your design process.

[3%] 4 min

14. Design a 5-input MUX with **tri-state enable** using only the functional block diagrams from the last two problems and if necessary the minimum number of SSI gates and tri-state buffers. The overall enable is E(L), the output is Y(H), the input(s) and select line(s) should be number subscripted as in our class notes and labs.