May the Schwartz be with you!

Exam 1

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Last Name, First Name

PropaGator 2: UF's PropaGator (Autonomous Surface Vehicle) for RoboBoat competition

Instructions:

- *Turn off all* ***cell phones*** *and other* ***noise making devices****.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for 33% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators, computers, or any electronic devices.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *Boolean expression answers must be in **lexical order**, (i.e., /A before A, A before B, & D_3 before D_2).*
- ***CLEARLY** write your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **13** distinct pages. Sign your name and add the date below. (If we struggle to read your name, you will lose points.)*
- *Failure to follow the below rules will result in **NO** partial credit*
  - *The **base** (radix) of all number should be indicated with a subscript or prefix.*
  - *Truth tables, voltage tables, and timing simulations must be in **counting** order.*
  - *Label the inputs and outputs of each circuit with activation-levels.*
  - *For each mixed-logic circuit diagram, label inputs of **each** gate with the appropriate logic equations.*
  - *For K-maps, label **each** grouping with the appropriate equation.*
  - *For each circuit design, equations must **not** be used as replacements for circuit elements.*
  - *Boolean expression answers must be in **lexical order**, (i.e., /A before A, A before B, & D_3 before D_2).*

PropaGator 2 front view

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

______________________________ SIGN YOUR NAME

______________ DATE (30 June 2015)

Regrade comments below: Give page # and problem # and reason for the petition.
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Problem	Available	Points
1	12	
2	14	
3	7	
4-5	11	
6	21	
7	5	
8	11	
9	10	
10	9	
TOTAL	100	

EEL 3701—Summer 2015
Tuesday, 30 June 2015

Dr. Eric. M. Schwartz

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[12%] 1. Solve the following arithmetic problems. **Remember to show ALL work here and in EVERY problem on this exam.**

(4%) 4 min

a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number **251_{10}**.

Binary: ____________________

Octal: ____________________

Hex: ____________________

BCD: ____________________

(3%) 2 min

b) Determine the **10-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number **-251_{10}**.

Signed Mag: ____________________

1's Comp: ____________________

2's Comp: ____________________

(2%) 3 min

c) What is **$511_{10} – 251_{10}$** in **10-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Remember that you must **show all work.** (Hint: 256+255=511) Please **circle** your answer.

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(3%) 1. d) What is $\mathbf{511_{10} + 251_{10}}$ in **<u>10-bit</u>** 2's complement and **<u>11-bit</u>** 2's complement? You must use binary numbers to **<u>derive</u>** and determine the solution (not decimal). Remember that you must **show <u>all</u> work.** Please **<u>circle</u>** your answers.

3 min

<u>10-bit</u> | **<u>11-bit</u>**

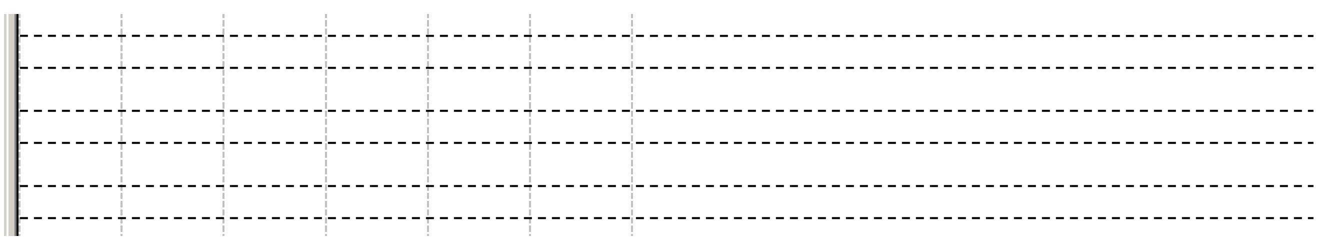
[14%] 2. Answer the following short questions. Show **<u>ALL</u>** work.

(4%) a) Draw a circuit like you would in a Quartus schematic entry [bdf] file to **DIRECTLY** implement (i.e., do **<u>NOT</u>** simplify) the equation Y = /(/A * B), where A is active-low, and B and Y are active-high. Use the **<u>minimum</u>** number of gates.

2 min

(3%) b) Draw a **<u>complete</u>** timing diagram, exactly as Quartus would; include 10ns propagation delays, as Quartus would. Label the inputs and output and the time axis.

3 min



(4%) c) Draw the required switch circuits and LED circuit to complete the circuit design for this problem. The circuits should do **nothing else**. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **<u>true</u>** positions.

2 min

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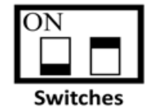
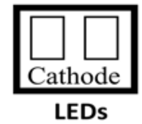
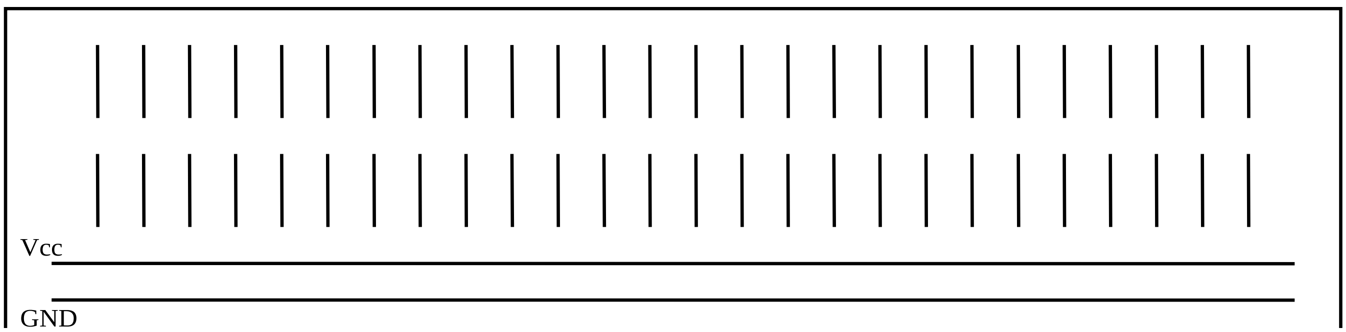
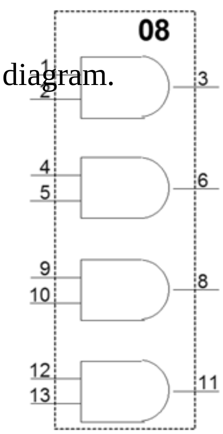
(3%) 5 min 2. d) Draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits** for **part c** and the logic from **part a**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don't know what chip you used, so assume whatever pin numbers you want (for the 14-pin chip), along with the **normal** power and ground pins. Label the pin numbers **in part a**. Label the wires for each of the inputs and outputs (A, B, and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions.







[7%] 5 min 3. Directly implement the below equation with a mixed-logic circuit diagram. (Do **NOT** simplify the equation.) Use only gates of the 74HC08 (or their mixed-logic equivalents). **Only if necessary**, you can also use other SSI components. Use the **minimum number of gates** required. Use the appropriate mixed-logic symbols. You are free to choose the activation levels that will optimize your solution. (No pin numbers are necessary.)



$$Soccer = \overline{\left[\,\overline{(G+\overline{O}\,)} * U\right] + \overline{S * \overline{A}}}$$

G( )___

O( )___

U( )___ _Soccer( )

S( )___

A( )___

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[4%] 5 min

4. Find the MSOP **or** MPOS equivalent of the below Boolean expression. Show **ALL** work. (Please verify that you are correctly reading the equation. Note that Ball, One and the second Num each have 3 bars above them.)

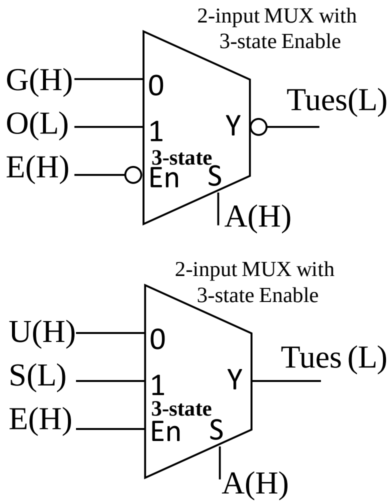
$$Gators = \overline{\left\{\left[UF + \overline{\left(Soft * \overline{Ball}\right)}\right] * \overline{\left(Num + \overline{One}\right)}\right\}} + \left[UF * \overline{\left(Base + \overline{Ball}\right) * \overline{\left(\overline{Num} + Three\right)}}\right]$$

Gators = _______________________

[7%] 5. What are the (SOP or POS) equations for the outputs of the following circuits? Lexical order is **NOT** necessary for these problems.

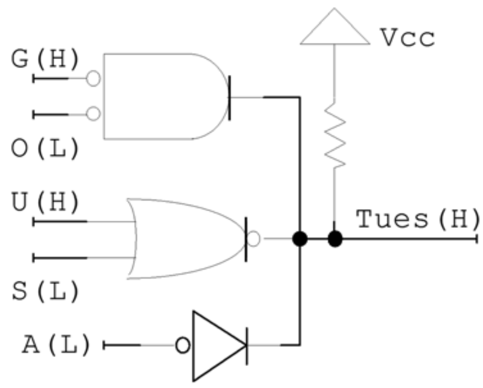
(4%) 4 min

a)



(3%) 4 min

b)



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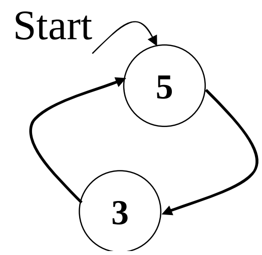
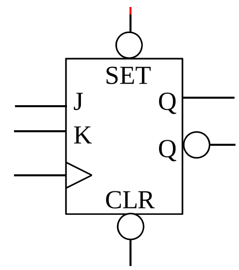
[21%] 6. Design a system that "counts" as shown with the values of **5**$_{10}$ and **3**$_{10}$. The system must **asynchronously** go to the state "5" when **Start** (**active-low**) goes true. Use a **T-FF** for the **least** significant bit of your design, a **JK-FF** for the next more significant bit (if necessary), and a D-FF(s) for **any other** bits you might need. The **least-significant "count" output** bit should be **active-high;** all **other "count" output** bits should be **active-low**. Note: All the given FFs have **asynchronous** clear and set inputs as shown.

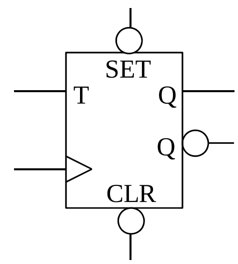
3 min

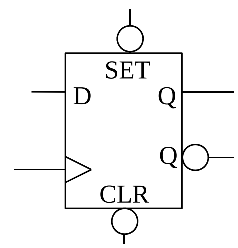


(a-d 10%) a) Draw a **functional block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your design in the dashed box with the inputs and outputs going **into or out of the box**, on the left or right, respectively. This is **not** a circuit diagram.

3 min







Inputs

Outputs

5 min

(a-d 10%) b) Complete the next-state **truth** table (**in counting order**).

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(a-d 10%) 6. c) Find the required **simplified** (MSOP or MPOS) equations.

3 min

(a-d 10%) d) Design the complete circuit, **minimizing** the total number of components, but using the T-FF, JK-FF, and D-FF(s) (if necessary), as described previously. All **inputs** and **outputs** of the circuit should be **clearly indicated** **coming into or out of** the below dashed box. Your design must include the circuitry necessary to **asynchronous** re-start the system at “**5**” when the **Start** (active-low) signal goes true.

5 min

Inputs

Outputs

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(e-f 4%) 4 min

6. e) Use the table in part b (or make a new table) to create the same counter, but this time use a **JK-FF** for the **<u>least</u>** significant bit of your design, a **T-FF** for the next more significant bit (if necessary), and a D-FF(s) for **any other** bits you might need. Find the required **<u>simplified</u>** (MSOP or MPOS) equations.

(e-f 4%) 4 min

f) Design the complete circuit as you did in part d, but this time for the design described in part e.

<u>Inputs</u> <u>Outputs</u>

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(g-i 7%) 6. g) Now add a **synchronous count** signal**, Count(H).** When **Count** is false, stop counting, just as you did you're your lab 5 counter when F and B were both false. Complete the next-state **truth** table (**in counting order**). Use a **JK-FF** for the **least** significant bit of your design, a **T-FF** for the next more significant bit (if necessary), and a D-FF(s) for **any other** bits you might need.

5 min

(g-i 7%) 6. h) Find the required **simplified** (MSOP or MPOS) equations.

5 min

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(g-i 7%) 6. i) Design the complete circuit as you did in part d and f, but this time for the design described in parts g-h.

4 min

Inputs

Outputs

[5%] 7. Use the below equation for this problem.

$$Y = (\bar{A} + \bar{B} + \bar{C})(\bar{A} + \bar{C})(A + B)(\bar{B})(B + C)$$

Use K-maps to simply the equation and put the result in MSOP **and** form MPOS.

5 min

A
BC

A
BC

Y_{MSOP} = ______________________________

Y_{MPOS} = ______________________________

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[12%] 8. Use the below equation for this problem.

$$Y = \bar{A}BCD + \bar{A}\bar{C}\bar{D} + A\bar{B}\bar{C} + A\bar{B}\bar{D} + ABD + \bar{B}C\bar{D} + B\bar{C}D$$

(6%) [7 min] a) Use K-maps to simply the equation and put the result in MSOP **and** form MPOS. Are these solutions (in part a) equivalent? Explain why or why not.

CD
AB ____________________

CD
AB ____________________

Y_{MSOP} =

Y_{MPOS} =

Equivalent?:

(5%) [3 min] b) If the terms ABCD=0001 and ABCD=1000, i.e., the textbook's d(1,8), are **DON'T CAREs (X)**, determine the new MSOP **and** MPOS equations. Are these solutions (in part b) equivalent? Explain why or why not.

CD
AB ____________________

CD
AB ____________________

Y_{MSOP} =

Y_{MPOS} =

Equivalent?:

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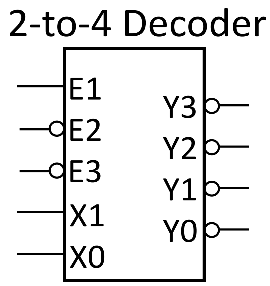
[10%] 7 min 9. Design a **3-to-8 Decoder** **with a single enable** using as many of the given **2-to-4 Decoders** with the enables (E1, E2, and E3) as necessary. Use the minimum number of **2-to-4 Decoders** and a minimum number of SSI (AND, NOR, NOT, etc.) gates necessary. (Note that all the enables on the **2-to-4 Decoders** must be true in order for the device to behave like a decoder.)



Inputs

Outputs

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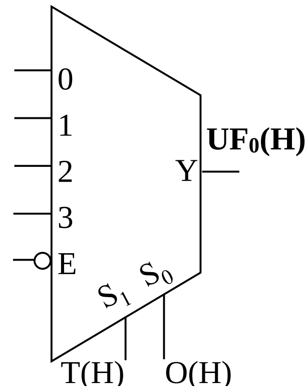
[9%] 2 min

10. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use the **minimum** number of additional SSI gates. Show all work. (The three below problems are **independent**.)

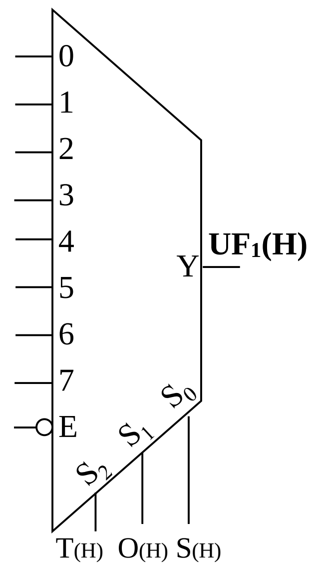
(4%) 4 min

a) **UF_0 = G*/A * (T*/O + O*/R*S + T*S)**



(3%) 3 min

b) **UF_1 = G*/A * (T*/O + O*/R*S + T*S)**



(2%) 3 min

b) **UF_2 = G*/A * (T*/O + O*/R*S + T*S)** (Note that the output is **active-low**.)