Exam 1

Last Name, First Name

May the Schwartz be with you!

Instructions:

- *Turn off all **cell phones** and other **noise making devices** and put away **all electronics**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "MORE ON BACK", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for 33% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators, computers, or any electronic devices.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- ***CLEARLY** write your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **11** distinct pages. Sign your name and add the date below. (If we struggle to read your name, you will lose points.)*
- *Failure to follow the below rules will result in **NO** partial credit*
  - *The **base** (radix) of all number should be indicated with a **subscript** or **prefix**.*
  - *Truth tables, voltage tables, and timing simulations must be in **counting** order.*
  - *Label the inputs and outputs of each circuit with activation-levels.*
  - *For each mixed-logic circuit diagram, label inputs of **each** gate with the appropriate logic equations.*
  - *For K-maps, label **each** grouping with the appropriate equation.*
  - *Labels inside of parts must be provided whenever it can be confusing, e.g., they **MUST** be specified for MUXes and Decoders, but not for NANDs and ORs.*
  - *For each circuit design, equations must **not** be used as replacements for circuit elements.*
  - *Boolean expression answers must be in **lexical order**, (i.e., /A before A, A before B, & D_3 before D_2).*

SubjuGator 8 CAD image for the 2016 RoboSub Competition.

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

SIGN YOUR NAME _____ DATE (28 June 2016) _____

Regrade comments below: Give page # and problem # and reason for the petition.
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Problem	Available	Points
1	12	
2	14	
3	7	
4	9	
5	4	
6	15	
7	18	
8	9	
9	12	
TOTAL	100	

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[12%] 1. Solve the following arithmetic problems. **Remember to show ALL work here and in EVERY problem on this exam.**

(4%) 4 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number $\mathbf{311_{10}}$.

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 2 min b) Determine the **10-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number $\mathbf{-311_{10}}$.

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(2%) 3 min c) What is $\mathbf{192_{10} - 311_{10}}$ in **10-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). You must **show all work.** (Hint: 128+64=192) Please **circle** your answer.

$(192_{10} - 311_{10})_2$ **10-bit 2's comp**: _____

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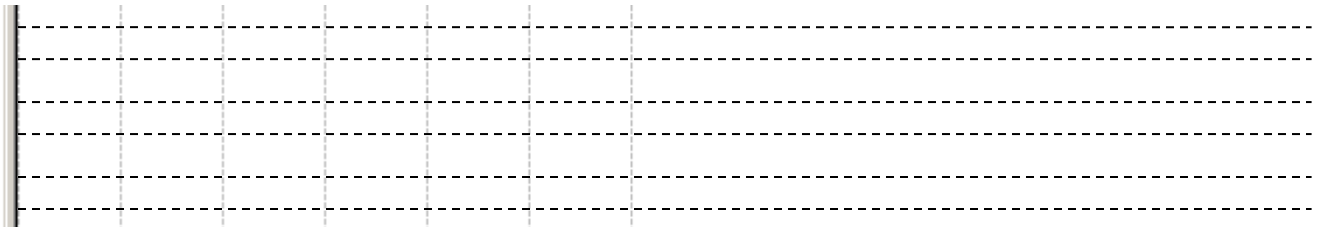
(2%) 3 min 1. d) What is **$-192_{10} - 311_{10}$** in **10-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). You must **show all work.**

$(-192_{10} - 311_{10})_2$ **10-bit 2's comp:** _____

[14%] 2. Answer the following short questions. Show **ALL** work.

(4%) 2 min a) Draw a circuit like you would in a Quartus schematic entry [bdf] file to **DIRECTLY** implement (i.e., do **NOT** simplify) the equation Y = /(/A + B), where A is active-high, and Y is active-low. B's activation level is intentionally unspecified, i.e., your choice. Use the **minimum** number of gates.

(3%) 3 min b) Draw a **complete** timing diagram, exactly as Quartus would; include 10ns propagation delays, as Quartus would. Label the inputs and output and the time axis.



(4%) 2 min c) Draw the required switch circuits and LED circuit to complete the circuit design for this problem. The circuits should do **nothing else**. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions.

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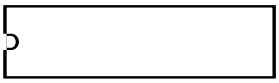
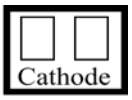
(3%) 5 min

2. d) Draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits** for **part c** and the logic from **part a**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don't know what chip(s) you used, so assume whatever pin numbers you want (for the 14-pin chip), along with the **normal** power and ground pins. Label the pin numbers **in part a**. Label the wires for each of the inputs and outputs (A, B, and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions.

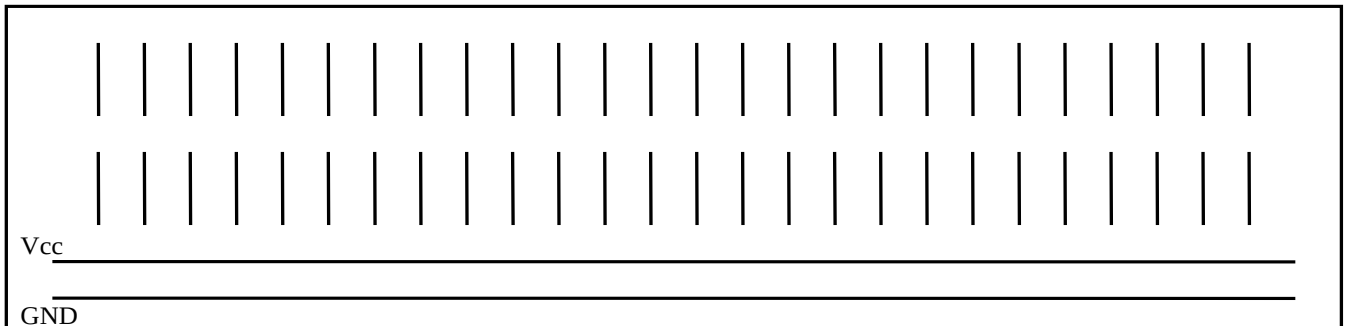


14-pin Chip

Switches



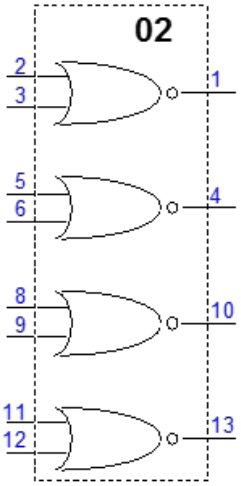
LEDs



[7%] 5 min

3. Directly implement the below equation with a mixed-logic circuit diagram. (Do **NOT** simplify the equation.) Use only gates of the 74HC02 (or their mixed-logic equivalents). **Only if necessary**, you can also use other SSI components. Use the **minimum number of gates** required. Use the appropriate mixed-logic symbols. You are free to choose the activation levels that will optimize your solution. (No pin numbers are necessary.)

$$Thx = \left\{\overline{[(B * \bar{A} + S) * E]} + \overline{\bar{B} + \bar{A} * L}\right\} * \mathrm{L}$$



B( )___

A( )___

S( )___

E( )___

L( )___

___*Thx*( )

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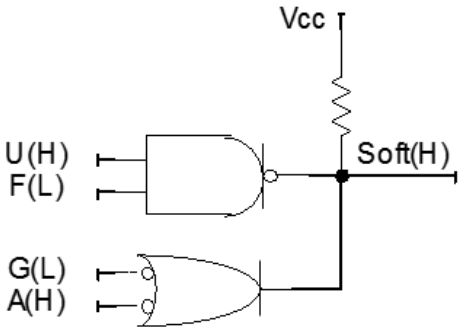
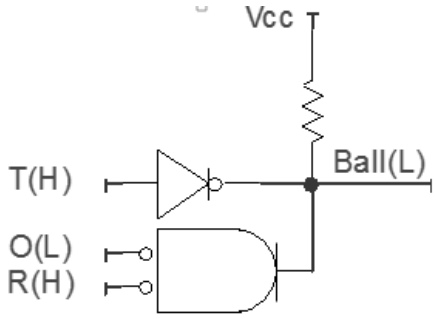
[7%] 4. What are the (SOP or POS) equations for the outputs of the following circuits? Please use lexical order.

(4%) 4 min a)



(3%) 4 min b)



(2%) 3 min c) What is the equation if the two outputs Soft and Ball are connected with a wire? Assume this combined signal is called **Go** and that it is active-high, i.e., **Go(H)**. Put this SOP or POS solution in lexical order.

[4%] 5 min 5. Find the MSOP **or** MPOS equivalent of the below Boolean expression. Show **ALL** work. (Please verify that you are correctly reading the equation.) Note that this equation is not identical to the equation in part 3.

$$Thx = \left\{\overline{\left[\overline{(B * \bar{A} + S)} * E\right]} + \overline{\bar{B} + \bar{A} * L}\right\} * L$$

Thx = _____

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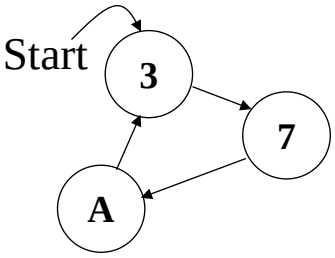
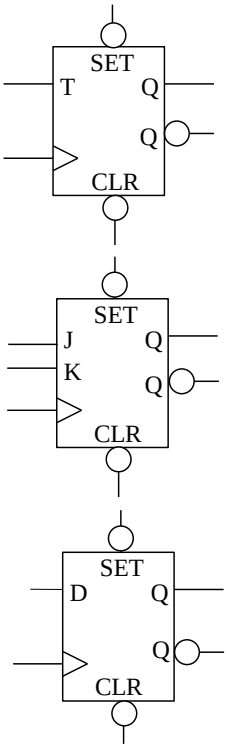
[15%] 6. Design a system that "counts" as shown with the values of **3_{16}**, **7_{16}** and **A_{16}**. 4-bits are output to represent these numbers. The system must **asynchronously** go to the state "3" when **Start** (**active-high**) goes true. Use a **T-FF** for the **most** significant bit of your design, a **JK-FF** for the **least** significant bit, and a D-FF(s) for **any other** bits you might need. An output, **Seven** (active-low), should be true if the "count" is "7." The **four "count" output** bits should all be **active-high**. Note: All the given FFs have **asynchronous** clear and set inputs as shown.



3 min

a) Draw a **functional block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your design in the dashed box with the inputs and outputs going **into or out of the box**, on the left or right, respectively. This is **not** a circuit diagram.



Inputs

Outputs

5 min

b) Complete the next-state **truth** table (**in counting order**).

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6. c) Find the required **simplified** (MSOP or MPOS) equations.

5 min

d) Design the complete circuit, **minimizing** the total number of components, but using the T-FF, JK-FF, and D-FF(s) (if necessary), as described previously. All **inputs** and **outputs** of the circuit should be **clearly indicated coming into or out of** the below dashed box. Your design must include the circuitry necessary to **asynchronous** re-start the system at "**3**" when the **Start** (active-high) signal goes true. The **Seven** (active-low) output must be true when the "count" is "7."

5 min

Inputs

Outputs

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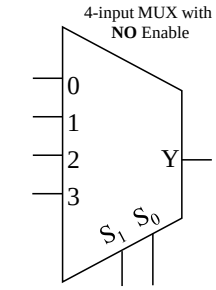
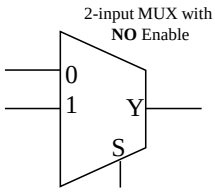
[18%] 7. Design the following multiplexers. The select lines must work as they normally do in selecting the proper MUX inputs.

(4%) 5 min

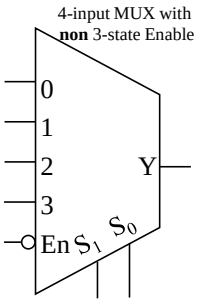
a) Design a **5-input MUX** with **no enable** using only MUXes of the two types given. Assume that a 4-input MUX costs 2.5 times more than a 2-input MUX. Design the minimum cost solution. If possible, use **nothing** else! (If this is not possible, use the minimum number of additional SSI gates.)

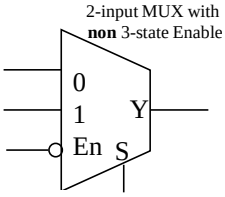




(4%) 5 min

b) Design a **5-input MUX** with **non 3-state enable** using only MUXes of the two types given. Assume that a 4-input MUX costs 2.5 times more than a 2-input MUX. Design the minimum cost solution. If possible, use **nothing** else! (If this is not possible, use the minimum number of additional SSI gates.)





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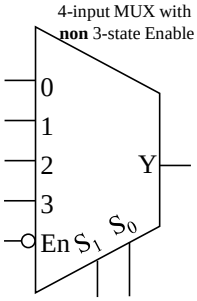
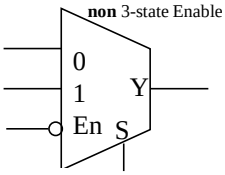
(5%) 7. c) Design a **6-input MUX** with **non 3-state enable** using only MUXes of the two types given. Assume that a 4-input MUX costs 2.5 times more than a 2-input MUX. Design the minimum cost solution. If possible, use **nothing** else! (If this is not possible, use the minimum number of additional SSI gates.)

5 min

4-input MUX with **non** 3-state Enable



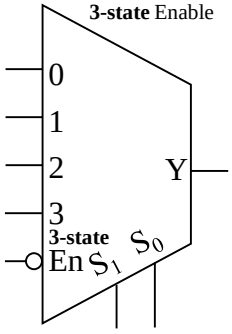
2-input MUX with **non** 3-state Enable



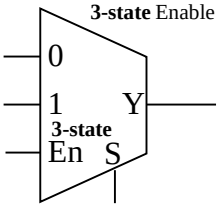
(5%) d) Design a **6-input MUX** with **NO** enable using only MUXes of the two types given. (Note that the activation-level of enable on the 2-input MUX has changed.) Assume that a 4-input MUX costs 2.5 times more than a 2-input MUX. Design the minimum cost solution. If possible, use **nothing** else! (If this is not possible, use the minimum number of additional SSI gates.)

5 min

4-input MUX with **3-state** Enable



2-input MUX with **3-state** Enable



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[9%] 8. Use the below equation for this problem.

$$Y = (\bar{A} + B + \bar{C} + D) * (\bar{A} + B + C) * (A + B + \bar{C} + \bar{D}) * (A + B + C) * (\bar{B} + C + \bar{D})$$

(5%) 7 min a) Use K-maps to simply the equation and put the result in MPOS **and** form MSOP. Are these solutions (in part a) equivalent? Explain why or why not.

CD / AB

CD / AB

Y_{MPOS} =

Y_{MSOP} =

Equivalent?:

(4%) 4 min b) If the terms ABCD=1000 and ABCD=1010, i.e., the textbook's d(8,10), are **DON'T CAREs (X)**, determine the new MPOS **and** MSOP equations. Are these solutions (in part b) equivalent? Explain why or why not.

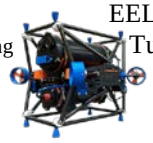
CD / AB

CD / AB

Y_{MPOS} =

Y_{MSOP} =

Equivalent?:



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SubjuGator

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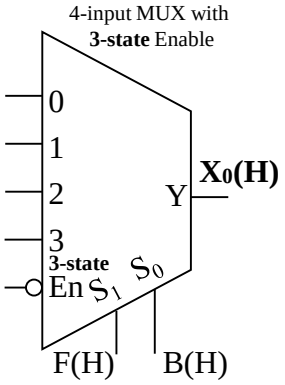
[12%] 9. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use the **minimum** number of additional SSI gates. Show all work. (The three below problems are **independent**.)

2 min

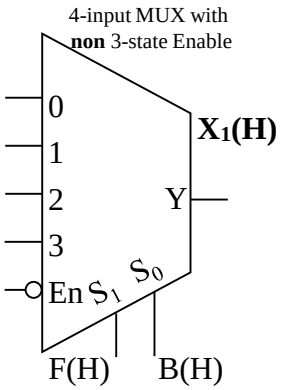
(4%) 4 min

a) $\mathbf{X_0} = \overline{(U + \bar{F})} * S + \overline{(U + \bar{B} + J)}$ = **/(U+/F) S + /(U + /B + J)**
Please note that the MUX has a **tri-state enable**.



(4%) 4 min

b) $\mathbf{X_1} = \overline{(U + \bar{F})} * S + \overline{(U + \bar{B} + J)}$ = **/(U+/F) S + /(U + /B + J)**
Please note that the MUX has a **NON** tri-state enable.



(4%) ~~3~~ min

c) $\mathbf{X_2} == \overline{(U + \bar{F})} * S + \overline{(U + \bar{B} + J)}$ = **/(U+/F) S + /(U + /B + J)**
Please note that **J is active-low** and the MUX has a **NON** tri-state enable.