Exam 1

Last Name, First Name

May the Schwartz be with you!

Instructions:

- *Turn off all **cell phones** and other **noise making devices** and put away **all electronics**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "**MORE ON BACK**", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for **33**% of your total course grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- ***CLEARLY** write your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **12** distinct pages. Sign your name and add the date below. (If we struggle to read your name, you will lose points.)*
- *Failure to follow the below rules will result in **NO** partial credit*
  - *The **base** (radix) of all number should be indicated with a **subscript** or **prefix**.*
  - *Truth tables, voltage tables, and timing simulations must be in **counting** order.*
  - *Label the inputs and outputs of each circuit with activation-levels.*
  - *For each mixed-logic circuit diagram, label inputs of **each** gate with the appropriate logic equations.*
  - *For K-maps, label **each** grouping with the appropriate equation.*
  - *Labels inside of parts must be provided whenever it can be confusing, e.g., they **MUST** be specified for MUXes and Decoders, but not for NANDs and ORs.*
  - *For each circuit design, equations must **not** be used as replacements for circuit elements.*
  - *Boolean expression answers must be in **lexical order**, (i.e., /A before A, A before B, & D_3 before D_2).*

Please read carefully.

Good luck & Go Gators!!!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

SIGN YOUR NAME _____ DATE (27 June 2017) _____

Regrade comments below: Give page # and problem # and reason for the petition.

Pages	Available	Points
2-3	18	
4	11	
5	10	
6-7	18	
8	14	
9	9	
10-11	12	
12	8	
TOTAL		

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[12%] 1. Solve the following arithmetic problems. **Remember to show <u>ALL</u> work here and in <u>EVERY</u> problem on this exam.**

(4%) 4 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number 437_{10}. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 4 min b) Determine the **<u>10-bit</u>** signed magnitude, 1's complement, and 2's complement representations of the decimal number -437_{10}. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(3%) 3 min c) What is $448_{10} - 437_{10}$ in 10-bit 2's complement? You must use binary numbers to **<u>derive</u>** and determine the solution (not decimal). Hint: $448 = 2^8+2^7+2^6$. You must **show <u>all</u> work.**

$(448_{10} - 437_{10})_2$ **10-bit 2's comp**: _____

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(2%) 1. d) What is -437_{10} in 11-bit 2's complement? You must **show <u>all</u> work.**

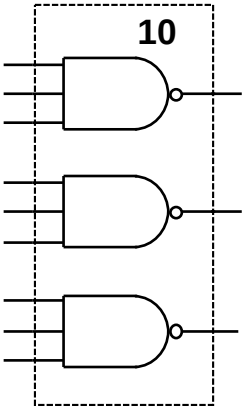
3 min

$(-437_{10})_2$ **11-bit 2's comp**:

[6%] 2. Directly implement the below equation with a mixed-logic circuit diagram, i.e., do **NOT** simplify the equation. Use only gates of the 74'10 (shown here) or their mixed-logic equivalents. Minimize the **total number of gates**. You are free to choose the activation levels that will optimize your solution. Check twice that you are correctly reading the equation!

5 min

$$UF = \overline{\overline{(B + A * \bar{S} + E)} + \overline{(B * \bar{A} + L)} + L}$$



B( )___

A( )___

S( )___

E( )___ _____UF( )

L( )___

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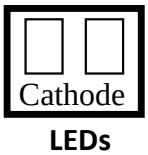
[11%] 3. Use the below circuit for this problem.

(5%) 4 min a) Draw the **mixed-logic circuit** diagram to directly implement the below two equations using parts any **one single chip**. Use the **minimum number of gates** from this single chip. (These should be **circuit diagrams,** not layout diagrams.)

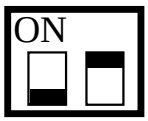
$$X = \overline{A * \bar{B}}$$
$$Y = \overline{\bar{A} + B}$$

(4%) 3 min b) Draw the required switch circuits and LED circuits to complete the circuit design for this problem. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions.

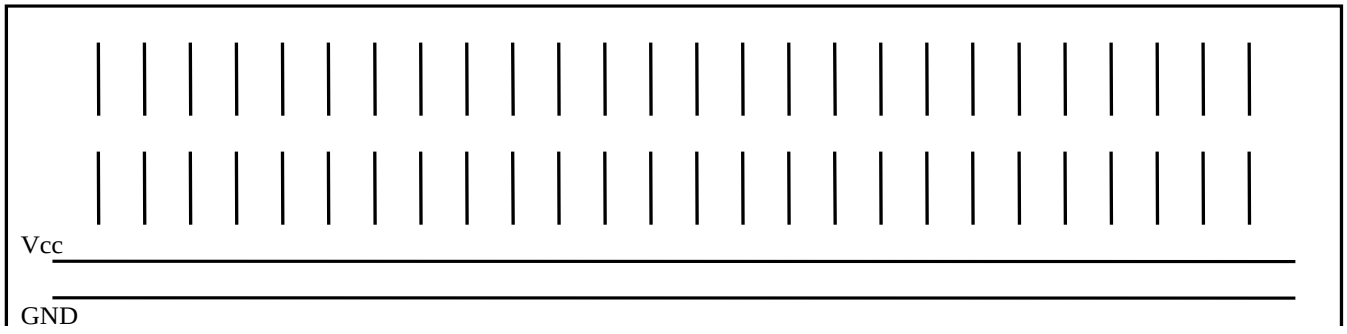
(2%) 6 min c) Draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits** from **part b** and the logic from **part a**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don't know what chip(s) you used, so assume whatever pin numbers you want (for the 14-pin chip), along with the **normal** power and ground pins. Label the pin numbers **in part a**. Label the wires for each of the inputs and outputs (A, B, X, and Y) with their activation levels. I suggest that you **use labels** to replace long wires. The dark part of the switches in the figure to the right are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions. For any other required parts, you may use any size parts that you need.



LEDs



Switches



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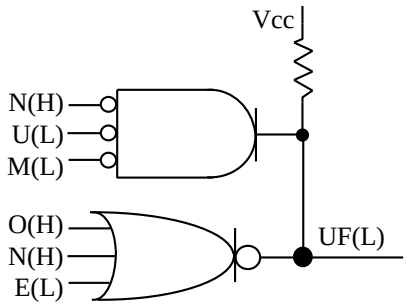
[4%] 5 min 4. **Simplify** the following logic equation using **only Boolean identities, laws or theorems**. Show all steps. Give the solution in MSOP or MPOS form.

$$Gator = \left[\overline{\left(\overline{S * \bar{O} + F}\right) * \bar{T}}\right] * \overline{\left(\overline{\bar{B} * A * \bar{L}} + \bar{L}\right)}$$

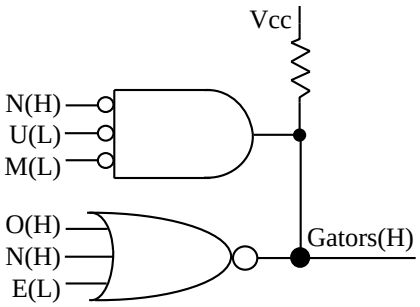
Gator = _____

[6%] 5 min 5. What are the (SOP or POS) equations for the outputs of the following circuits? For this problem, you do **NOT** need to use lexical order. Do **NOT** simplify.

a)



b)



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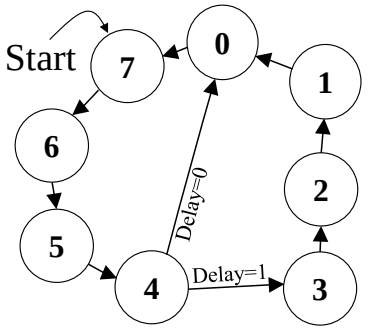
[18%] 6. Design a system that normally counts down as follows 7, 6, 5, 4, 0, 7, 6, …, when the Delay(L) is false. But if Delay(L) is true, then three more count values are inserted between 4 and 0, i.e., the count sequence 7, 6, 5, 4, **3, 2, 1,** 0, 7, 6, …. The system must **asynchronously** go to state "7" when **Start** (**active-high**) goes true. Use a **D-FF** for the **most** significant bit of your design, a **JK-FF** for the **least** significant bit, and T-FF(s) for **any other** bits you might need. An **active-low** output, **Hold** should be true when the count is 3, 2, or 1. All other outputs (including the state bits) should be **active-high**. Note: All the given FFs have **asynchronous** clear and set inputs as shown.

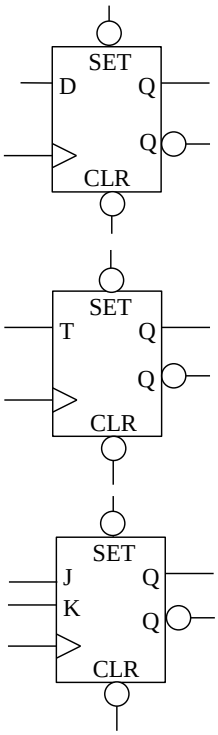


4 min

( )

a) Draw a **functional block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your functional blocks of your design in the dashed box with the inputs and outputs going **into or out of the box**, on the left or right, respectively. This is **not** a circuit diagram.

4 min



Inputs

Outputs

6 min

( )

b) Complete the next-state **truth** table (**in counting order**).

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( ) 4 min

6. c) Find the **simplified** (MSOP or MPOS) equations for $\mathbf{K_0}$ (from the JK-FF) and **Hold**. Find an SOP or POS equation for $\mathbf{J_0}$ (from the JK-FF, which does **NOT** need to be simplified). You do **NOT** need to find **any of the other** equations.

( ) 6 min

d) Design the complete circuit, **minimizing** the total number of components, but using the D-FF, JK-FF(s), and T-FF(s), as described previously. All **inputs** and **outputs** of the circuit should be **clearly indicated coming into or out of** the below dashed box. Draw empty boxes for combinatorial equations not required and not found. Your design must include the circuitry necessary to **asynchronous** go to count 7 when **Start** (**active-high**) goes true.

Inputs

Outputs

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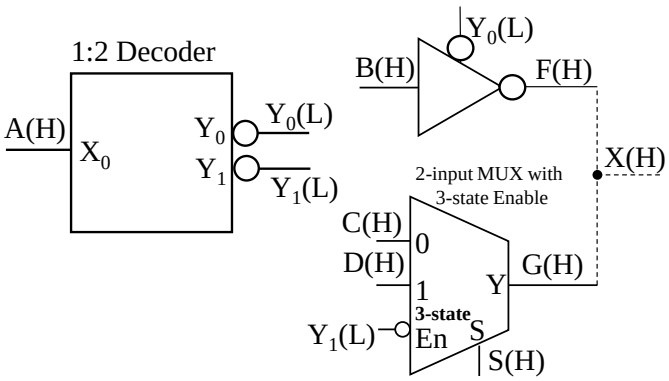
[8%] 10 min 7. Determine each of the below equations **in lexical order**. For parts a through c, assume that the dashed line is **not there**.



(1%) a) $Y_0 = f_1(A)$ and $Y_1 = f_2(A)$.

Y_0 =

Y_1 =

(2%) b) $F = f_3(B, Y_0)$

F =

(2%) c) $G = f_4(C, D, Y_1, S)$

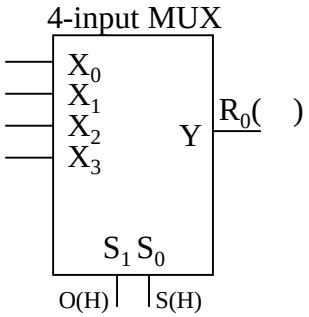
G =

(3%) d) If F(H) and G(H) are connected (as shown with the dashed lines) and the combined signal is called X(H), what is the equation for $X = f_5(A, B, C, D, S)$.

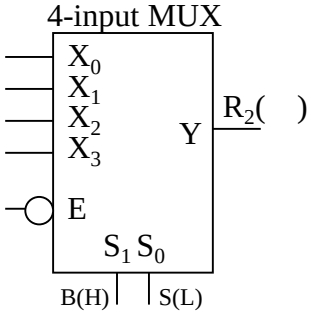
X =

[6%] 2 min 8. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use only SSI gates and add the **minimum** number necessary. Show all work. (The below two problems are **independent**.)

(%) 5 min a) $\boldsymbol{R_0 = \overline{(O + \overline{B})} + (\overline{O} * T)S}$



(%) 3 min b) $\boldsymbol{R_2 = \overline{(O + \overline{B})} + (\overline{O} * T)S}$ (Note the **NON** tri-state enable.)



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[9%] 9. Use the below equation for this problem.

$$Y = (\bar{A} + \bar{B} + \bar{C} + \bar{D}) * (\bar{A} + \bar{B} + C + D) * (\bar{A} + B + C) * (\bar{A} + B + D) * (\bar{A} + C + \bar{D}) * (A + B + \bar{C} + D) * (A + \bar{B} + \bar{D})$$

(8%) 7 min a) Fill in the below K-maps for finding the MPOS (on the left) **and** MSOP (on the right). Put **DON'T CARE (X)** in the ABCD=0010 and 1011 locations, i.e., the textbook's d(2) and d(11). Now determine the MPOS and MSOP equations

AB
CD

AB
CD

Y_{MPOS} =

Y_{MSOP} =

(1%) 1 min b) Are the above equations **equivalent**? Why or why not?

_____

_____

_____

_____

_____

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[12%] 10. Solve the below problems.

(1%) 3 min a) Draw a **functional block diagram** of a **1-bit full adder circuit** with inputs A, B, and C_{IN} (carry input). The outputs are SUM and C_{OUT} (carry out). The equations for the full adder are as follows (where ⊕ means Exclusive-OR),

Sum = A ⊕ B ⊕ Cin
Cout = A*B + A*Cin + B*Cin

(2%) 3 min b) Draw a functional block diagram, derive a **truth table**, and **design a 1-bit equivalence circuit**, i.e., **`EQ = A equiv B`** (`EQ = 1` if and only iff `A=B`) using **ONLY** gates from the following list: AND, BAND, NAND, BNAND, OR, BOR, NOR, BNOR, and NOT.

(2%) 3 min c) Draw a **functional block diagram** for a **1-bit ALU** with the functions in the below table. Note that for addition, there is both a carry input (C_{IN}) and a carry output (C_{OUT}).

S1	*S0*	*Function*
0	*0*	*A or B*
0	*1*	*not B*
1	*0*	*A plus B plus CIN*
1	*1*	*A equiv B*

(4%) 4 min

10. d) Design the 1-bit ALU described above using **ONLY** SSI or MSI gates. Functional block diagrams from parts a and b should be used instead of the circuit designs of parts a and b. For other parts of the design, use circuit elements. The C_{OUT} in this design should equal 0 unless addition is used, and in that case it should be equal to the C_{OUT} from the adder.

(3%) 3 min

e) Design a 2-bit ALU using described above using **ONLY** previous designs in this problem. Functional block diagrams in parts a, b, and c should be used instead of the circuits designed circuits. The C_{OUT} in this design should equal 0 unless addition is used, and in that case it should be equal to the C_{OUT} from the adder.

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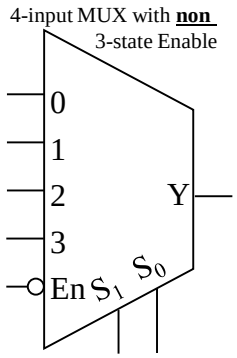
[8%] 11. Design the following multiplexers. The select lines must work as they normally do in selecting the proper MUX inputs.

(4%) 5 min a) Design a **6-input MUX with a non 3-state enable** using only MUXes of the type given. Design the minimum cost solution, i.e., use as few of these MUXes as possible. If possible, use **nothing** else! (If this is not possible, use the minimum number of additional SSI gates.) The active-high inputs are X_J, the active-high select lines are S_K, the active-low **non** tri-state enable is E, and the active-high output is Y.



(4%) 5 min b) Design an **8-input MUX with a tri-state** enable using only MUXes of the type given. Design the minimum cost solution, i.e., use as few of these MUXes as possible. If possible, use **nothing** else! (If this is not possible, use the minimum number of additional SSI gates.) The active-high inputs are X_J, the active-high select lines are S_K, the active-low **tri-state** enable is E, and the active-high output is Y.