Exam 1

13-Feb-19 -- 1:13 PM

May the Schwartz be with you!

Last Name, First Name

Instructions:

- *Turn off all **cell phones** and other **noise making devices** and put away **all electronics**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "**MORE ON BACK**", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *You may not use any notes, HW, labs, other books, scratch paper, or calculators.*
- *This exam counts for **30**% of your total course grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- ***CLEARLY** write your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **12** distinct pages. Sign your name and add the date below. (If we struggle to read your name, you will lose points.)*
- *For anything undefined, if necessary, state a reasonable assumption.*
- *Failure to follow the below rules will result in **NO** partial credit*
  - *The **base** (radix) of all number should be indicated with a **subscript** or **prefix**.*
  - *Truth tables, voltage tables, and timing simulations must be in **counting** order.*
  - *Label the inputs and outputs of each circuit with activation-levels.*
  - *For each mixed-logic circuit diagram, label inputs of **each** gate with the appropriate logic equations.*
  - *For K-maps, label **each** grouping with the appropriate equation.*
  - *Labels inside of parts must be provided whenever it can be confusing, e.g., they **MUST** be specified for MUXes and Decoders, but not for NANDs and ORs.*
  - *For each circuit design, equations must **not** be used as replacements for circuit elements.*
  - *Boolean expression answers must be in **lexical order**, (i.e., /A before A, A before B, & D_3 before D_2).*

SubjuGator in 2018

Good luck!

Happy 4th!

Please read carefully.

Go Gators!

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

SIGN YOUR NAME _____ DATE (3 July 2018) _____

Regrade comments below: Give page # and problem # and reason for the petition.

Pages	Available	Points
2-3	19	
4	10	
5	9	
6	12	
7	12	
8-9	16	
10-11	14	
12	8	
TOTAL	100	

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[19%] 1. Solve the following arithmetic problems. **Remember to show ALL work here and in EVERY problem on this exam.**

(4%) 4 min a) Determine the unsigned hexadecimal, octal, binary, and BCD representations of the number 567_{10}. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Binary: _____

Octal: _____

Hex: _____

BCD: _____

(3%) 4 min b) Determine the **12-bit** signed magnitude, 1's complement, and 2's complement representations of the decimal number -567_{10}. (I **strongly** recommend that you **check your work before** moving on to the next problem.)

Signed Mag: _____

1's Comp: _____

2's Comp: _____

(2%) 3 min c) What is -567_{10} in **11-bit** 2's complement? You must use binary numbers to **derive** and determine the solution (not decimal). Hint: $2048 = 2^{11}$, $1024 = 2^{10}$, and $512 = 2^{9}$. You must **show all work.**

$-567_{2\ 11\text{-bit 2's comp}}$: _____

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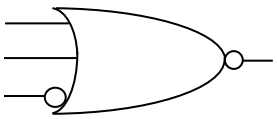
(3%) 1. d) What is $-567_{10} - 567_{10}$ in **11-bit** 2's complement? You must **show all work.**
3 min

$(-567_{10} - 567_{10})_{2\text{ 11-bit 2's comp}}$: _____

[6%] 2. Directly implement the below equation with a mixed-logic circuit diagram, i.e., do **NOT** simplify the equation. Use only gates of the type shown here (or their mixed-logic equivalents). Minimize the **total number of gates**. You are free to choose the activation levels that are not already specified and that will optimize your solution. Check twice that you are correctly reading the equation!
6 min



$$UF = \overline{\left\{\left[(I + \bar{S}) * \overline{T * \bar{H} * E}\right] * B\right\} + E * \overline{(S + \bar{T})}}$$

I( )____

S(**H**)____

T(**L**)____

H( )____ __UF( )

E(**H**)____

B(**L**)____

E(**H**)____

S(**H**)____

T(**L**)____

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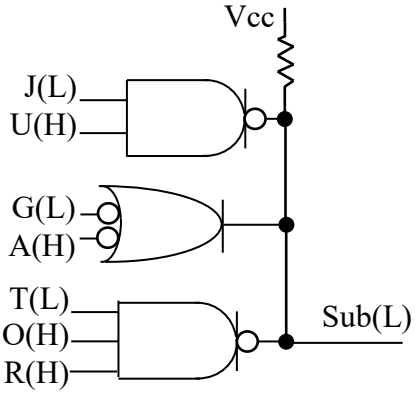
[4%] 6 min 3. **Simplify** the following logic equation using **only Boolean identities, laws or theorems**. (Note that this equation is **NOT** the same as in the previous problem. Show all steps. Give the solution in MSOP or MPOS form.

$$UF = \overline{\left\{\left[(I + \bar{S}) * \overline{T * \bar{H} * E}\right] * B\right\}} + \left[B + E * \overline{(S + \bar{T})}\right]$$

[6%] 4. What is the (SOP or POS) equation for the output of the circuit for part a? For this problem, you do **NOT** need to use lexical order. Do **NOT** simplify.

(4%) 5 min a)



(2%) 2 min b) If possible, add a single **SSI** (**not** MSI, i.e., not an open-collector gate) gate to design a circuit for

$$\boldsymbol{Go = V * \bar{F} * Sub},$$

where Go and Sub are active-low. If not possible, add the minimum number of additional SSI gates.

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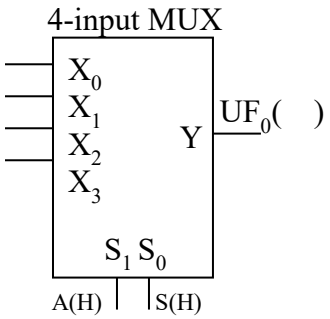
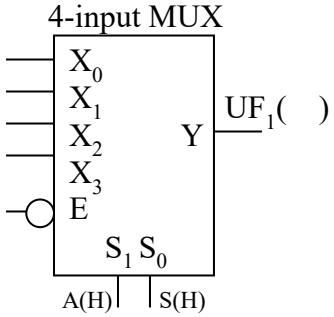
[9%] 2 min 5. Use the given multiplexers to **design mixed-logic circuit diagrams** that solve each of the below problems. **Be careful to read the equation correctly.** Choose activation levels for each signal (that has not already been assigned) to **minimize** the number of additional parts required. Use only SSI gates and add the **minimum** number necessary. Show all work. (The three below problems are **independent**, but the equations are identical.)

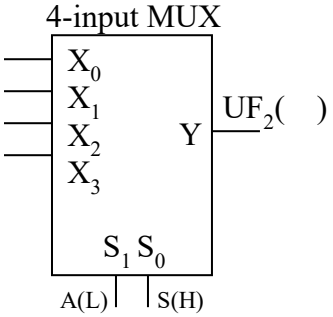
(4%) 6 min a) $\boldsymbol{UF_0 = B * (\bar{A} + S) + [B * (A + L)] * L}$



(3%) 3 min b) $\boldsymbol{UF_1 = B * (\bar{A} + S) + [B * (A + L)] * L}$ (Note the **NON** tri-state enable.)



(2%) 4 min c) $\boldsymbol{UF_2 = B * (\bar{A} + S) + [B * (A + L)] * L}$ (**No enable!**)



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[12%] 6. Use the below equation for this problem.

$$Y = (\bar{A} + \bar{B} + \bar{C} + \bar{D}) * (\bar{A} + B + C) * (\bar{A} + B + D) * (A + \bar{B} + \bar{D}) * (A + B + C + \bar{D}) * (B + \bar{C} + \bar{D})$$

(8%) 8 min a) Simply the above equation and put the result in MPOS **and** MSOP form.

AB / CD

AB / CD

Y_{MPOS} =

Y_{MSOP} =

(3%) 4 min b) If the term ABCD=1111, i.e., the textbook's d(15), are **DON'T CARE (X)**, determine the new MSOP and MPOS equations

AB / CD

AB / CD

Y_{MPOS} =

Y_{MSOP} =

(1%) 1 min c) Are the above equations (in part b) **equivalent**? Why or why not?

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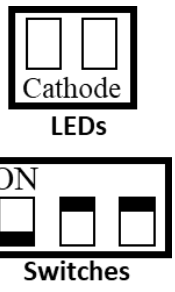
[12%] 7. Use the below circuit for this problem.

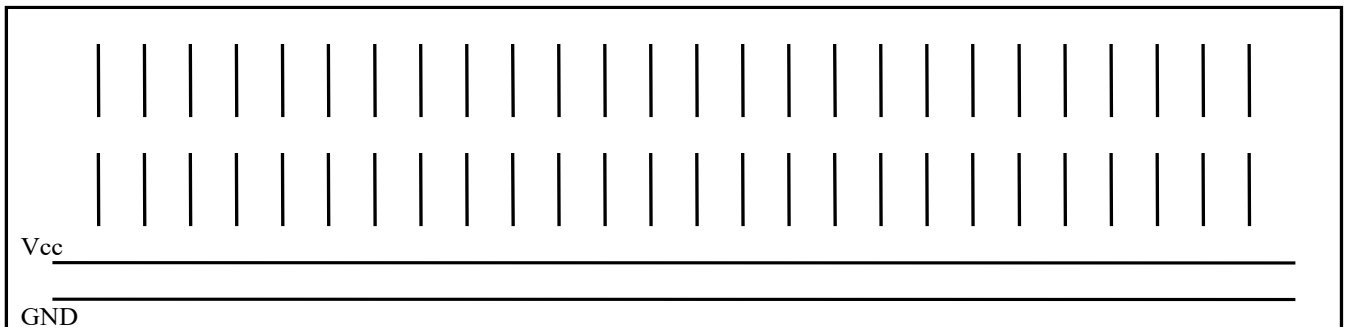
(5%) 5 min a) Draw the **mixed-logic circuit** diagram to directly implement (i.e., do **NOT** simplify) the below equation using parts from any **one single chip**. Use the **minimum number of gates** from this **single** chip. (This should be a **circuit diagram,** not a layout diagram.)

$$X = \overline{\bar{A} + \overline{B * \bar{C}}}$$

(4%) 3 min b) Draw the required switch circuits and LED circuits to complete the circuit design for this problem. (These should be **circuit diagrams,** not layout diagrams.) Draw the switches in their **true** positions.

(3%) 5 min c) Draw a **layout** of the entire above circuit **including** each of the **switch and LED circuits** from **part b** and the logic from **part a**. A layout shows each of the parts as they appear on the breadboard. Include the needed switches, resistors (SIP and/or DIP), and LEDs. I don't know what chip(s) you used, so assume whatever pin numbers you want (for the 14-pin chip), along with the **normal** power and ground pins. Label the pin numbers **in part a**. Label the wires for each of the inputs and outputs (A, B, C, and X) with their activation levels. I suggest that you **use labels** to replace crossing wires. The dark part of the switches in the figure to the right are the parts that you move to change the switch's closure state. Draw the switches in their **true** positions. For any other required parts, you may use any size parts that you need.





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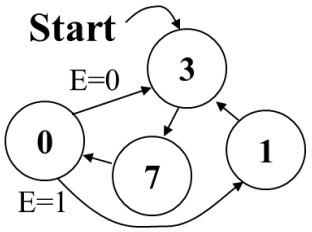
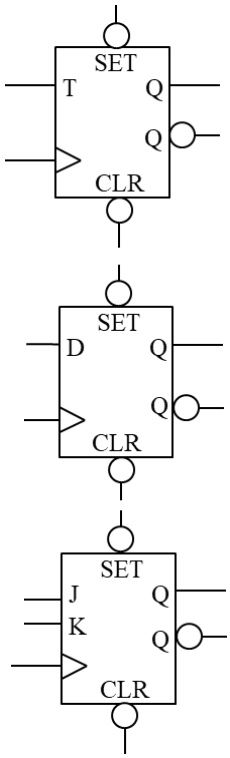
[16%] 8. 2 min Design a system that "counts" as shown. The system must **asynchronously** go to state "3" when **Start** (**active-low**) goes true. **E** (extend) is an active-high signal that determines the next "count" after "0," as shown in the figure. Use a **T-FF** for the **most** significant bit of your design, a **JK-FF** for the **least** significant bit, and **D-FF**(s) for **any other** bits you might need. An **active-high** output, **Yay** should be true when the "count" is "1." All other outputs should be **active-high**. Note: All the given FFs have **asynchronous** clear and set inputs as shown.



(2%) 4 min a) Draw a **functional block diagram** (showing **all** the inputs, **all** the outputs, and the functional blocks). Put your design in the dashed box with the inputs and outputs going **into or out of the box**, on the left or right, respectively. This is **not** a circuit diagram.

Inputs

Outputs



(7%) 6 min b) Complete the next-state **truth** table (**in counting order**).

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(3%) 5 min 8. c) Find the required **simplified** (MSOP or MPOS) equations for **J**, **K**, and **Yay**. For the other equations, you do **not** need MSOP or MPOS equations, but you must provide correct SOP or POS for each.

(4%) 5 min d) Design the complete circuit, using the T-FF, D-FF(s), and JK-FF(s), as described previously. All **inputs** and **outputs** of the circuit should be **clearly indicated coming into or out of** the below dashed box. For non-required circuits, use a box specifying inputs and outputs. Your design must include the circuitry necessary to **asynchronous** go to state "**3**" when **Start** (**active-low**) goes true.

Inputs

Outputs

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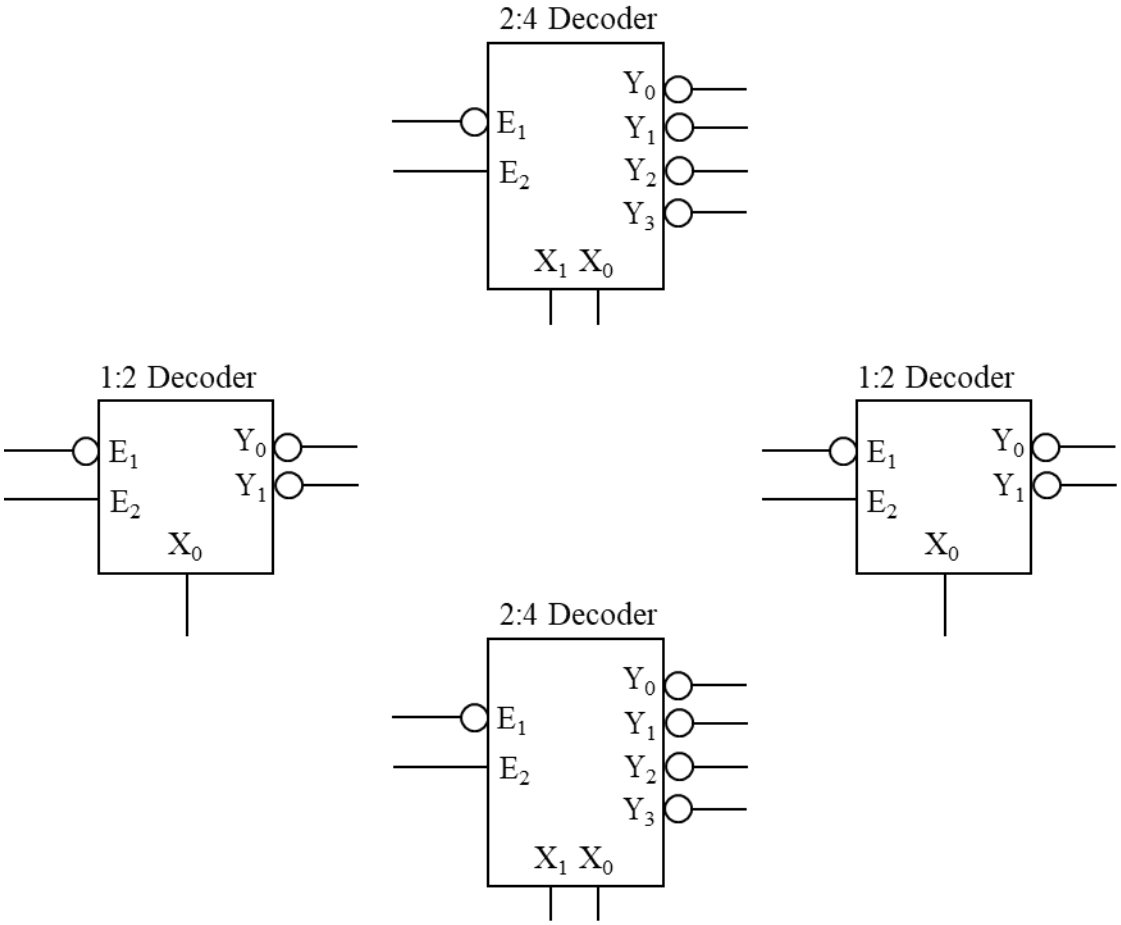
[14%] 9. In this problem you will design a 3-to-8 decoder with a single active-high enable. Two 2-to-4 and two 1-to-2 decoders, all with two enables, one active-high and one active-low, are shown below.

(1%) 2 min

a) Draw a functional block diagram of a **3-to-8 decoder with a single active-high enable, E**. The other inputs ($\mathbf{X_J}$) must be active-high and the outputs ($\mathbf{Y_K}$) must be active-low.

(8%) 6 min

b) Design the **3-to-8 decoder with a single active-high enable** below, using **only** the below parts. (If you can **not** solve it this way, add additional necessary parts.)



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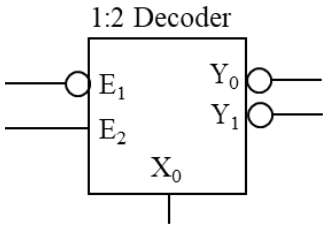
(1%) 9. c) Draw a functional block diagram of the **1-to-2 decoder** shown here (and used in the previous problem).

2 min



(4%) d) Design the **1-to-2 decoder** of parts b and c using **only** SSI components. Show **ALL** your work.

4 min

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[8%] 10. In this problem you will design an 8-input multiplexer with a single active-low tri-state enable.

2 min Two 4-input multiplexers, each with three **tri-state** enables (one active-high and two active-low), are shown below. Two 2-input multiplexers, each with two tri-state enables (one active-high and one active-low), are shown.

(1%) a) Draw a functional block diagram of an **8-input multiplexer with a single active-low tri-state enable**. All other inputs and outputs are active-high. The inputs are X and S (with subscripts), the output is Y.

2 min

(7%) b) Design the **8-input multiplexer with a single active-low tri-state enable**. Use the **minimum number** of the parts below. (If you can **not** solve it this way, add additional necessary parts.)

7 min