Exam 2

Last Name, First Name

May the Schwartz be with you!

UF's potential entry for 2016 Maritime RobotX.

Please read carefully.

Good luck & Go Gators!!!

Instructions:

- *Turn off all **cell phones** and other **noise making devices** and put away **all electronics**.*
- *Show **all** work on the **front** of the test papers. **Box** each answer. If you need more room, make a clearly indicated note on the front of the page, "**MORE ON BACK**", and use the back. The back of the page will **not** be graded without an indication on the front.*
- *This exam counts for 20% of your total grade.*
- *Read each question **carefully** and **follow the instructions**.*
- *You may **not** use any notes, HW, labs, other books, or calculators.*
- *The point values for problems may be changed at prof's discretion.*
- *You must pledge and sign this page in order for a grade to be assigned.*
- *Put your name at the top of **this** test page (and, if you remove the staple, all others). Be sure your exam consists of **11** distinct pages. Sign your name and add the date below.*
- *Failure to follow the below rules will result in **NO** partial credit*
  - *The base (radix) of all number should be indicated with a subscript or prefix.*
  - *Truth tables, voltage tables, and timing simulations must be in counting order.*
  - *Label the inputs and outputs of each circuit with activation-levels.*
  - *For each mixed-logic circuit diagram, label inputs of each gate with the appropriate logic equations.*
  - *For K-maps, label each grouping with the appropriate equation.*
  - *Labels inside of parts must be provided whenever it can be confusing, e.g., they MUST be specified for MUXes and Decoders, but not for NANDs and ORs.*
  - *For each circuit design, equations must not be used as replacements for circuit elements.*
  - *Boolean expression answers must be in lexical order, (i.e., /A before A, A before B, & D3 before D2).*

PLEDGE: On my honor as a University of Florida student, I certify that I have neither given nor received any aid on this examination, nor I have seen anyone else do so.

SIGN YOUR NAME _____ DATE (13 November 2014) _____

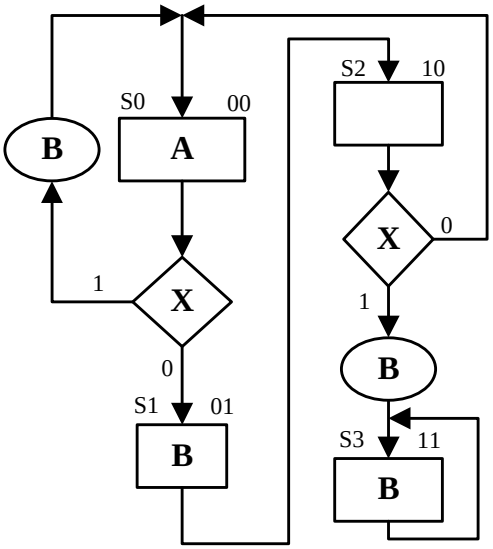
Regrade comments below: Give page # **and** problem # and reason for the petition.
.
.
.
.
.
.
.
.
.

Page	Available	Points
2-3	15	
4	20	
5-6	22	
7-8	20	
9-10	15	
11	8	
TOTAL	100	

Exam 2

Last Name, First Name _____

[15%] 1. In this problem you will ultimately design a circuit to implement this ASM. Use only SSI gates, a **JK-FF** for the **most significant state bit**, a **T-FF** for the **least significant state bit**, and D-FF's for any other FF's that you might need. The signals **X** and **B** are **active-low** and **A** is **active-high**. An active-high signal (**Go**) should **asynchronously** move the machine to state **S1**.



3 min

(%) a) Complete the next-state **truth** table. You may **not** need all the rows and/or columns.

5 min

(%) b) Find the required **simplified** (MSOP or MPOS) equations.

5 min

Exam 2

Last Name, First Name

(%) 1. c) Design the complete mixed-logic circuit diagram, **minimizing** the total number of components, but using the JK-FF and T-FF (and D-FF(s), if necessary) as described previously. All **inputs** and **outputs** of the circuit should be **clearly indicated coming into or out of** the below box. Your design must include the circuitry necessary to **asynchronously** cause the system to go to state S1 when the **Go** (active-high) signal goes true. For debugging purposes, **also output the active-low** versions of the **state bits**.

5 min

Inputs **Outputs**

Exam 2

Last Name, First Name

[6%] 2. Answer the following questions about a state machine designed with one EEPROM, one J-K flip-flop, one T flip-flop, and any other necessary flip-flops of type D.

(3%) 3 min a) What is the size of the EEPROM (addresses × data bits) if the state machine has 3 inputs, 10 outputs, and 4 states? Provide numbers only, i.e, 37×9, **NOT** expressions like $3^7 \times \sqrt[4]{37}$.

(3%) 3 min b) What is the size of the EEPROM (addresses × data bits) if the state machine has 3 inputs, 4 outputs, and 11 states? Provide numbers only, i.e, 37×9, **NOT** expressions like $3^7 \times \sqrt[4]{37}$.

[4%] 4 min 3. Draw a complete mixed-logic circuit diagram **including two switch circuits**, one for an **active-high** input signal, **X(H)** and one for an **active-low** input, **Y(L)**, to generate the equation $W = \overline{X + \overline{Y}}$. Draw the switches in their **true** positions. Draw an **LED circuit** for the **active-low** output, **W(L)**. Do **NOT** draw a layout.

[5%] 4. Answer the following short VHDL-related questions.

(2%) 1 min a) Write the complete VHDL equation (one line) for $W = \overline{X + \overline{Y * Z}}$.

(2%) 1 min b) In VHDL, what does 0 mean? What does 1 mean?

(1%) 1 min c) In VHDL, what are the two major components of all VHDL files?

[5%] 5. Answer the following short questions.

[3%] 2 min a) Why is was a Mealy output required in the traffic light controller of lab 7. Be specific.

(2%) 2 min b) Can we get the same result (for all practical purposes) without using a Mealy output? If so, how?

Exam 2

Last Name, First Name

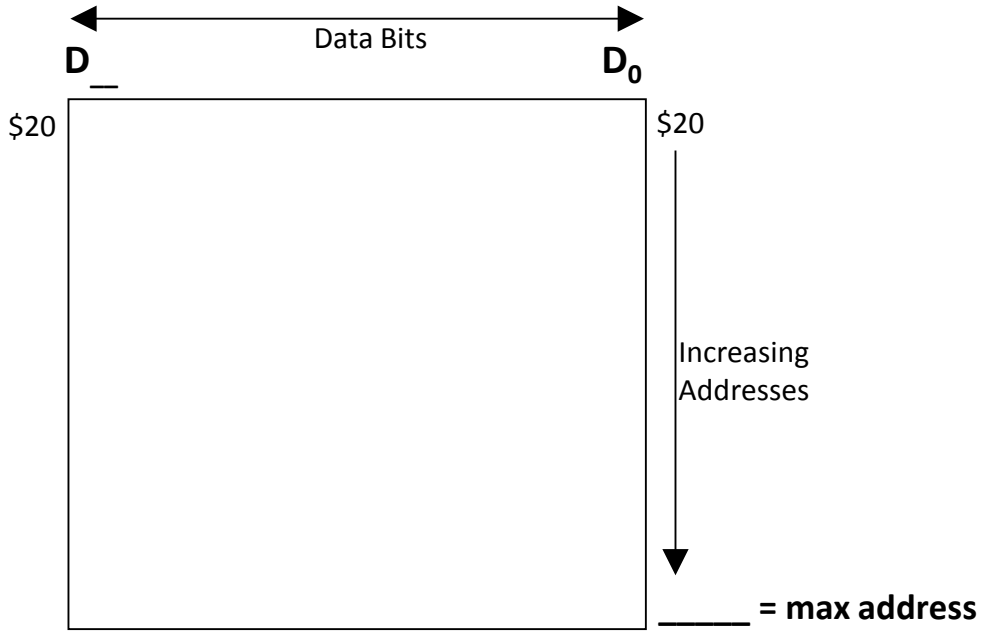
[22%] 6. Given as many of each of the following as needed, design the memory module described below, with an **active-low** chip enable, **CE(L)**: **64×8 SRAMs**, **32×4 EEPROMs**, and **64×4 FLASH EEPROMs**, The device should begin at address **$20 = 20_{16}** with a **64x8 SRAM**, followed immediately by a 64x8 block made up of **64×4** of **FLASH AND 64×4** of **EEPROM**. Immediate follow this memory block with a **32×8** block of **EEPROM**. Add the **minimum number** of memory devices and the **minimum number** of additional **SSI** components required, i.e., other than the memory, **no** other MSI or LSI components are allowed.)

3 min

(%)

a) Draw vertical and horizontal lines in the box below and label each resulting box with the memory type and size, using only the defined types and sizes given above. Also, fill in the subscript on the D at the top left and the maximum address at the bottom right.

5 min



(%)

b) What are the address and data ranges for **each of the** memory components drawn above (in **binary** and in **hex**)?

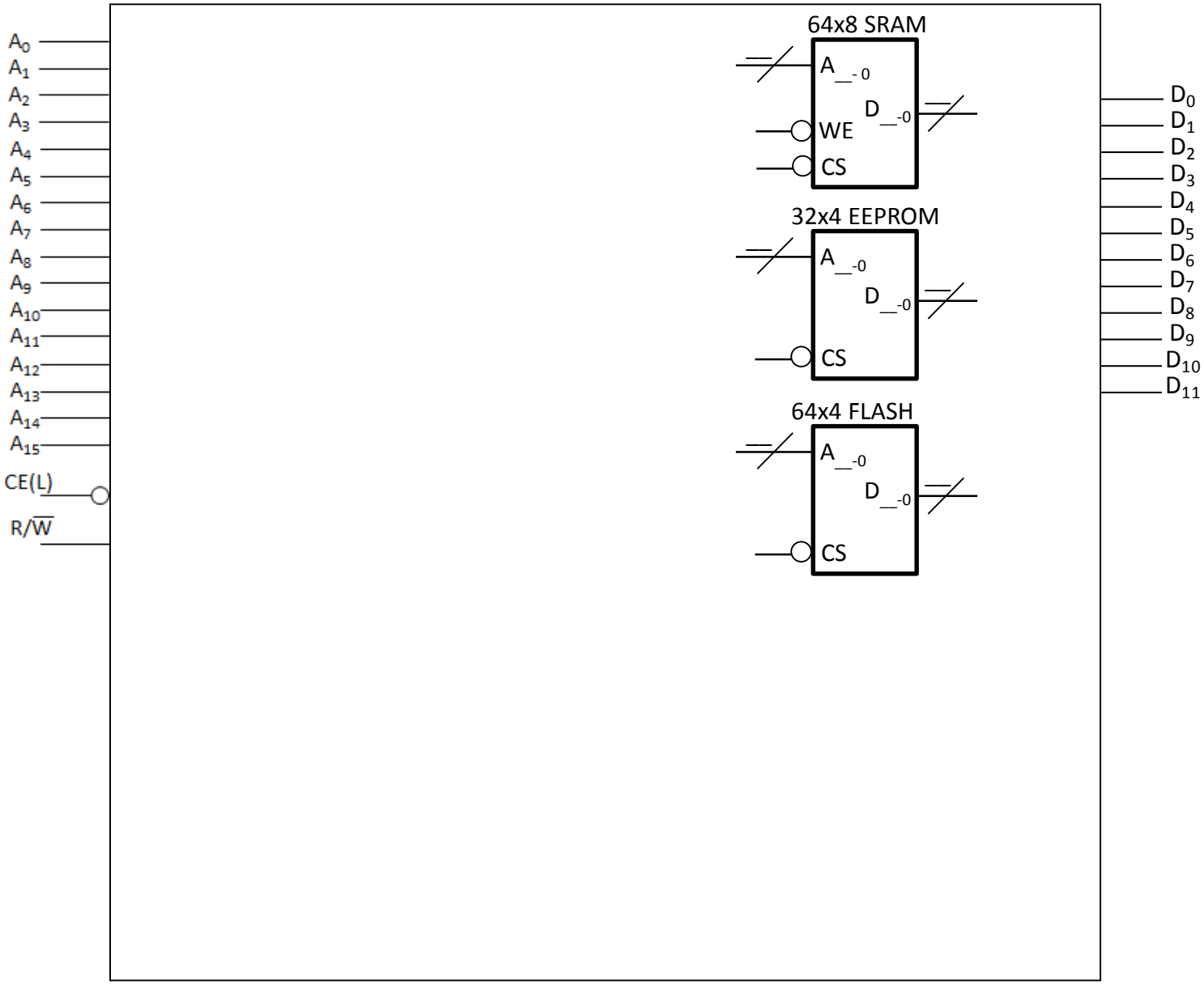
6 min

Exam 2

Last Name, First Name

(%) 6. c) Design the required memory device circuit diagram below. Add the **minimum number** of **additional** memory components and SSI **gates** necessary (**no** MSI gates, LSI gates or PLDs). **Add** memory components and address and data subscripts as needed; **cross out** unneeded address and data pins. **Use labels instead of wires for the design**. **Also**, **write the equations** for each CS at the bottom of the page. Show **all connections** with either labels or wires (**labels are preferred**), just as in Quartus. Don't forget the system's **active-low** chip enable, **CE,** and **R/~W** [pronounced "read, write not," with R(H) and W(L)].

8 min



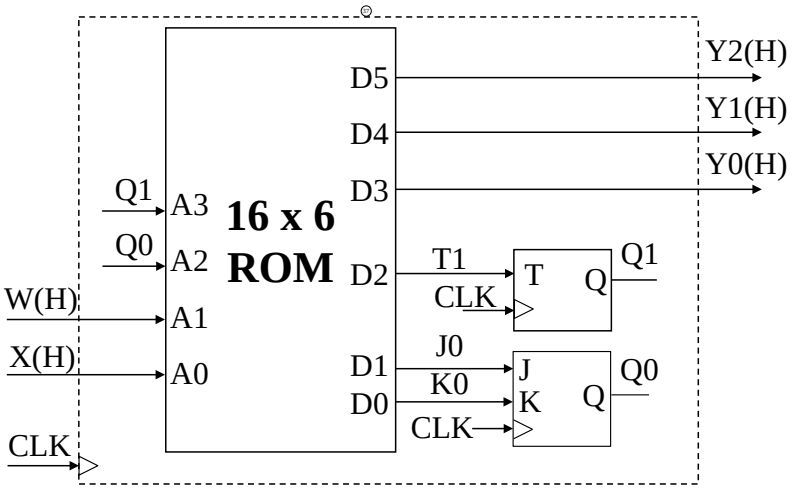
Equations:

Exam 2

Last Name, First Name

[20%] 7. Use the below circuit diagram and the **ROM contents table** below to solve this problem. Note that the addresses and data in the table are in **hexadecimal** [base 16]. (This problem is very similar to a problem in homework 8 that was also done in class.) Note that a T-FF and a JK-FF are utilized in the below circuit.

(16%) 17 min a) **Derive** the ASM chart for this circuit. Show **ALL** work, i.e., use at least part of the below table. You can draw your ASM on this page or on the next page.



					Contents of ROM (Hex)												
					Addr	**Data**											
					0	**23**											
					1	**05**											
					2	**22**											
					3	**04**											
					4	**17**											
					5	**15**											
					6	**1E**											
					7	**1C**											
					8	**1B**											
					9	**19**											
					A	**1B**											
					B	**19**											
					C	**02**											
					D	**21**											
					E	**17**											
					F	**0D**											

Exam 2

Last Name, First Name

(16%) 7. a) (**Repeated** from previous page.) **Derive** the ASM chart for this circuit. Show **ALL** work, i.e., use at least part of the above blank table. You can draw your ASM on this page or on the previous page.

(2%) 3 min b) If the input X is active-low, explain how this will change the ASM (if at all). Do **NOT** redraw the ASM.

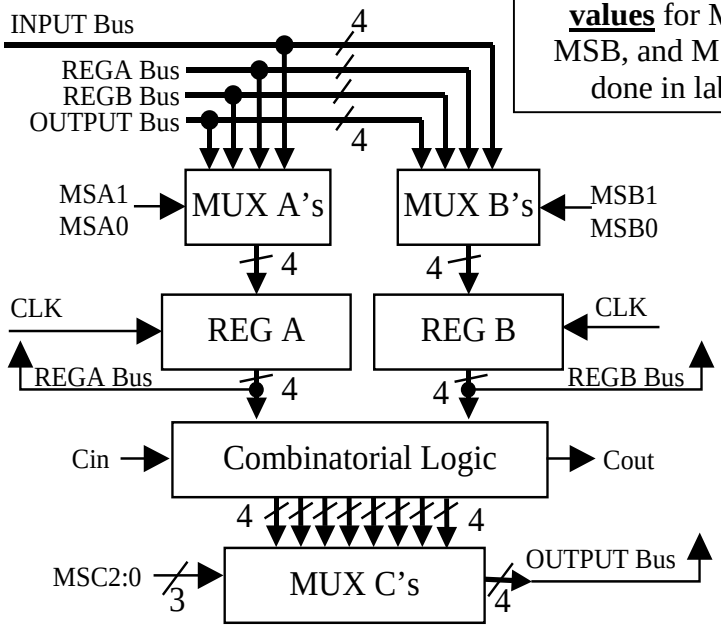
(2%) 4 min c) If the outputs are all active-low, **redraw the state S_0 (00) of the ASM**. Do **NOT** redraw the **entire** ASM, just redraw the **entire** first state. (This problem is independent from part b, i.e., X is still active-high.)

Exam 2

Last Name, First Name

[15%] 8. A block diagram of your lab 6 is shown here, along with two tables from the same handout.

3 min



Use **proper default values** for MSA, MSB, and MSC, as done in lab 6.

MSA1:0/ MSB1:0	Bus Selected as Input to Combinatorial Logic
00	INPUT Bus
01	REG A Bus
10	REG B Bus
11	Output Bus

MSC	Action
000	REGA Bus to OUTPUT Bus
001	REGB Bus to OUTPUT Bus
010	complement of REGA Bus to OUTPUT Bus
011	bit wise AND REGA/REGB to OUTPUT Bus
100	bit wise OR REGA/REGB Bus to OUTPUT Bus
101	sum of REGA Bus & REGB Bus to OUTPUT Bus
110	shift REGA Bus left one bit to OUTPUT Bus
111	shift REGA Bus right one bit to OUTPUT Bus **without** sign extension

(5%) 5 min

a) Assume that you can add a small additional circuit to calculate when REGA is equal to three (0011_2) and REGB is equal to seven (0111_2). Design a circuit for each of these active-high outputs (**Aeq3** and **Beq7**) and a third output when both are true (**ABeq37**). Show **ALL** work.

Exam 2

Last Name, First Name

(5%) 5 min

8. b) Find the average of two numbers (use 3 and 7), and put the results in register A. Describe what is accomplished in each step. Use the minimum number of clock cycles. Give appropriate values for **ALL** signals. (Your algorithm should still work even if the two numbers are changed.)

#	MSA	MSB	MSC	Input	Cin	RegA	RegB	Output	Cout	RegA+	RegB+	Output+	Cout+
1						0100	0010						
2													
3													
4													
5													
6													
7													

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____

(5%) 5 min

c) Subtract the value in B from the value in A, i.e., **A – B**, and put the results in register B. If this is not possible, then say so. Use the values presently in A and B, i.e., 7 and 3. Describe what is accomplished in each step. Use the minimum number of clock cycles. Give appropriate values for **ALL** signals. (Your algorithm should still work even if the two numbers are changed.)

#	MSA	MSB	MSC	Input	Cin	RegA	RegB	Output	Cout	RegA+	RegB+	Output+	Cout+
1						0111	0011						
2													
3													
4													
5													
6													
7													

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____

Exam 2

Last Name, First Name

[8%] 9. Answer the following short questions.

SpaceX Dragon's capsule.

(3%) 3 min

a) There were recently two private rocket companies that experienced catastrophic crashes with their vehicles. Space Exploration Technologies Corporation (SpaceX), an employer of many UF graduates, has yet to have a major problem. Assume an FSU or a UGA graduate were on the payroll of Orbital Sciences Corp and/or The Spaceship Company, both of which had tragic accidents in the last few weeks. Describe how the rocket countdown (10, 9, 8, 7, 6, …, 1, 0) can be influenced by a noisy clock signal. How can this be prevented?

(2%) 3 min

b) Assume that you are using a **circuit design** for problem 6 (on pages 5-6) that was created by an **FSU graduate**. After running a **program** (that reads and writes values to the memory devices) written by a **Georgia graduate**, you note that **programs that you previously wrote and ran successfully on the FSU-designed board** no longer work, i.e., perfectly written code (by a UF student or graduate) ran perfectly on the FSU-designed board, but an imperfect Georgia program damaged (BOOM!) the FSU-designed board. Suggest a likely errors for the Georgia code and for the FSU design.

(3%) 3 min

c) Al Gore gave the manufacturers at Fracture™ (who print photographs directly on glass) the idea for this Gainesville-based company. A new feature that I envision for the glass images is to **instantly** self-destruct (with several tiny explosives) when a crack is detected (from a digital input), in order to protect from major injuries. Al Gore likes to save power, and therefore has very slow clock speeds on all of his state machines. What must be done in the state machine to protect customers?

Al Gore's Image on a glass table top.