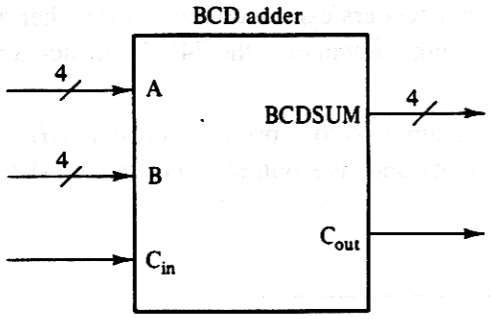


74'85

Figure 4.25 BCD adder for Problem 4.5.

4.6. Using 74'85 comparators, design a 16-bit magnitude comparator.

4.7. Design the 4-bit magnitude comparator of Fig. 4.26, using a 74'85 comparator plus any additional gates that are needed. Note that this comparator has three more than the usual number of outputs. These are <=, >=, and <>, which represent less than or equal to, greater than or equal to, and not equal to, respectively.

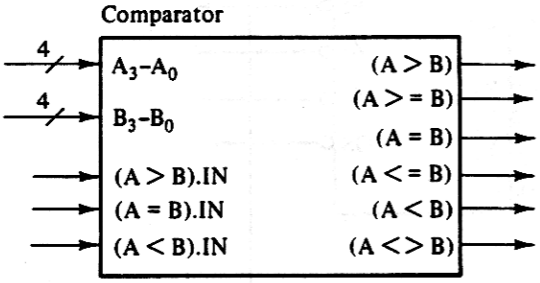


Figure 4.26 Comparator for Problem 4.7.

4.8. Design a 5-to-32 decoder using 74'138 decoders and any additional gates that are required.

4.9. Given an 8-bit address A_7–A_0, what are the addresses that will enable the modules M_0, M_1, M_2, and M_3 shown in Fig. 4.27. For convenience, use X for a don't-care address bit.

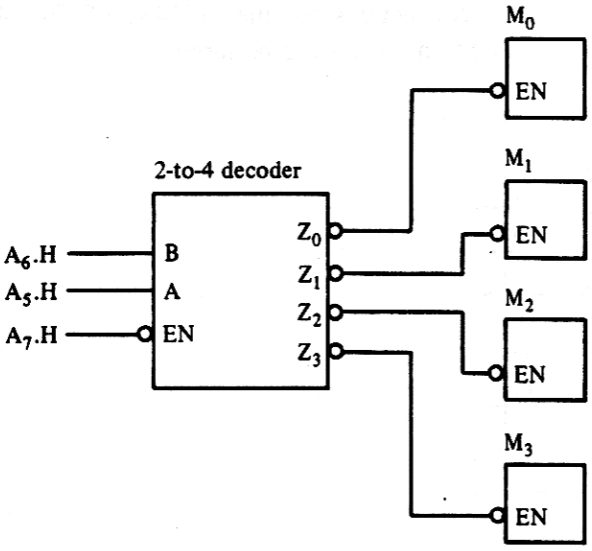


Figure 4.27 Circuit for Problem 4.9.

4.10. Using the truth table for a BCD-to-7-segment decoder shown in Fig. 4.11(c), derive the logic equations for the seven outputs a, b, c, d, e, f, and g.

4.11. A chain of 74'47 BCD-to-7-segment decoders can be connected together as shown in Fig. 4.12(c) to display leading zeros as blanks. Reconnect the 74'47s in such a way that leading zeros are displayed as zeros.

4.12. Design Module M in Fig. 4.28 to obtain a 16-to-4 priority encoder. (*Hint:* Module M is a combinational circuit with eight inputs and five outputs. You are to determine the logic equations for the five outputs.)

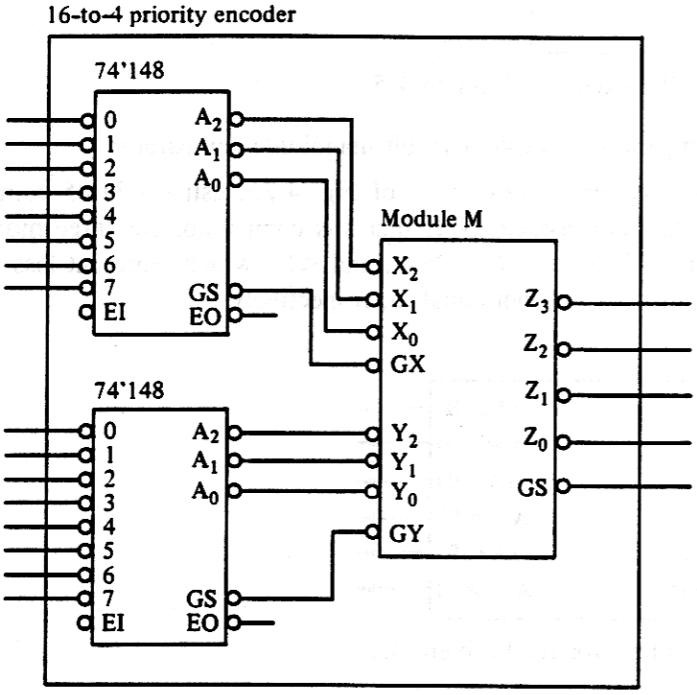
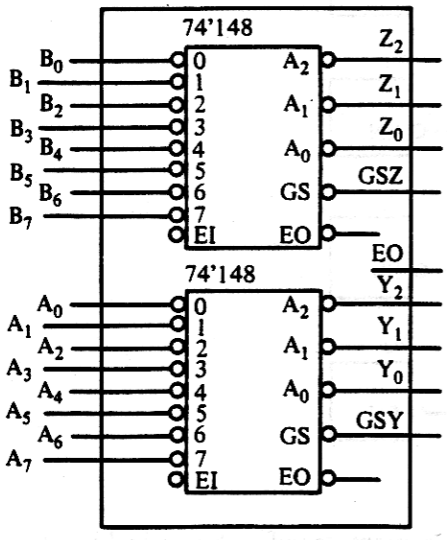


Figure 4.28 Encoder for Problem 4.12.

4.13. The enable output EO and enable input EI of a 74'148 can be used to cascade 74'148 priority encoders for easy octal expansion. Such an expansion for the 74'148s of Fig. 4.29(a) is shown in Fig. 4.29(b). Show connections for the 74'148s of Fig. 4.29(a) that will accomplish this expansion. No additional gates are required.



(a)

EI	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	Z_2	Z_1	Z_0	Y_2	Y_1	Y_0	GSZ	GSY	E0
0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	X	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
1	X	X	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0
1	X	X	X	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0
1	X	X	X	X	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
1	X	X	X	X	X	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0
1	X	X	X	X	X	X	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0
1	X	X	X	X	X	X	X	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0
1	X	X	X	X	X	X	X	X	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	X	X	X	X	X	X	X	X	X	1	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
1	X	X	X	X	X	X	X	X	X	X	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0
1	X	X	X	X	X	X	X	X	X	X	X	1	0	0	0	0	0	1	1	0	0	0	1	0	0
1	X	X	X	X	X	X	X	X	X	X	X	X	1	0	0	0	1	0	0	0	0	0	1	0	0
1	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	0	1	0	1	0	0	0	1	0	0
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	1	1	0	0	0	0	1	0	0
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	1	1	0	0	0	1	0	0

(b)

Figure 4.29 Table and components for Problem 4.13.

4.14. **(a)** Determine the complete truth table for the four-input MUX shown in Fig. 4.16.
(b) Derive the logic equation for Z.

4.15. In Fig. 4.20, a 16-input MUX is realized with 4 four-input MUXs and a decoder. But, suppose no decoder is available. Design a 16-input MUX using any number of 4-input MUXs (74'253), but no decoders.

4.16. Using a 74'148 priority encoder and any additional gates that are required, design the circuit of Fig. 4.30 for generating the S_0 and S_1 control inputs for the circuit of Fig. 4.18. Each of the requesting devices (A, B, C, and D) can request a connection to device X through the signals REQA, REQB, REQC, and REQD, respectively. If there are competing requests, then the order of priority is as follows: D, C, B, and A, with D having the highest priority. If no request is made, then device X is connected to A by default.

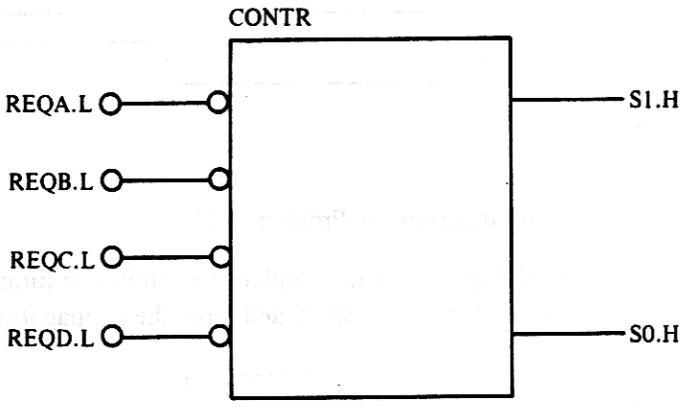


Figure 4.30 Circuit for Problem 4.16.

4.17. Design the circuit BIDIR of Fig. 4.31 such that the signal DATA is bidirectional. Specifically, when IOCTR is 1 (H), then DATA is connected to INPUT and the direction of the data flow is "in." But when IOCTR is 0 (L), then DATA is connected to OUTPUT and the direction of the data flow is "out." (*Hint:* Use 74'125 three-state logic elements.)

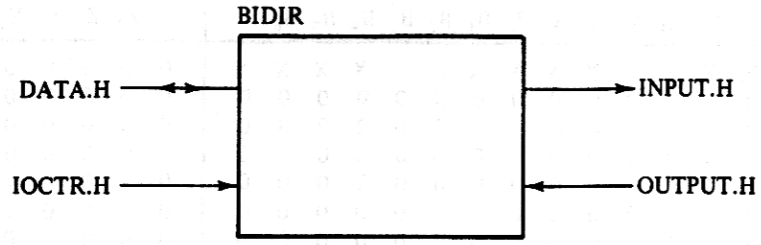


Figure 4.31 Circuit for Problem 4.17.

4.18. **(a)** Discuss the similarities and the differences between a decoder and a demultiplexer.
(b) An encoder performs the inverse function of a decoder, and a multiplexer performs the inverse function of a demultiplexer. Then, is there any relationship between an encoder and a multiplexer? Explain.

4.19. What is the maximum number of standard-TTL inputs that an ALS-TTL output can drive?

4.20. If the signal MEMCS shown in Fig. 4.32 activates the CS inputs of a bank of memory chips with the specified characteristics, how many CS inputs can it safely drive?

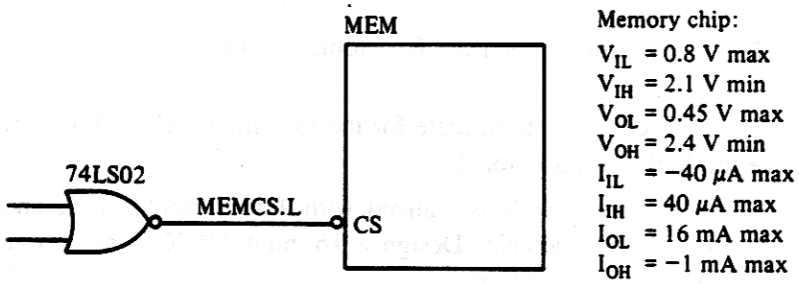


Figure 4.32 Circuit for Problem 4.20.

4.21. What is the noise margin for the ALS-TTL series components?

4.22. If an ALS-TTL output drives a number of LS-TTL inputs, what is the resultant noise margin?

4.23. Given the Exclusive OR gate of Fig. 4.33(a), complete the shown timing diagram for Z in Fig. 4.33(b). Be sure to show and label the propagation delays t_{pHL} and t_{pLH}.

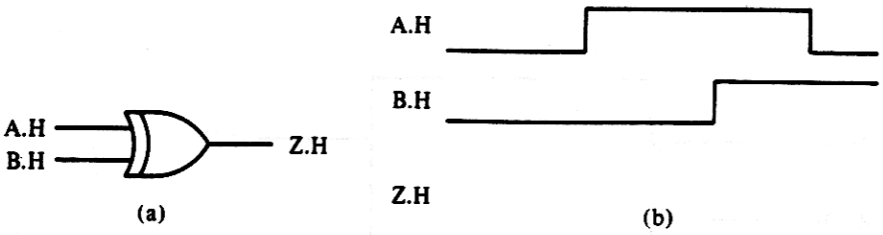


Figure 4.33 Gate and timing diagram for Problem 4.23.

4.24. Given the circuit diagram of Fig. 4.34(a), complete the shown timing diagram in Fig. 4.34(b) for the signals $\overline{A}$ and Z. Be sure to show and label the propagation delays t_{pHL} and t_{pLH}.

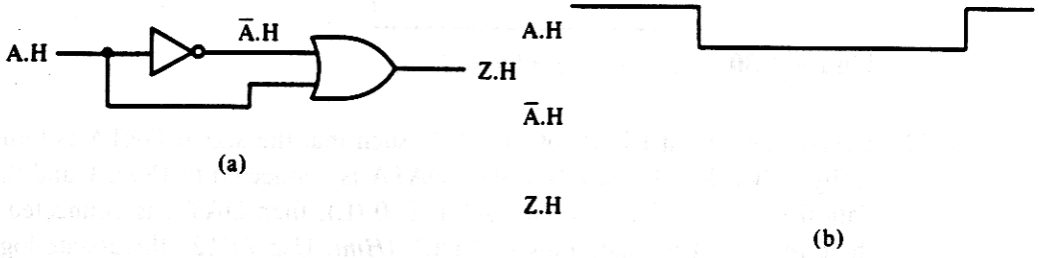


Figure 4.34 Gate and timing diagram for Problem 4.24.