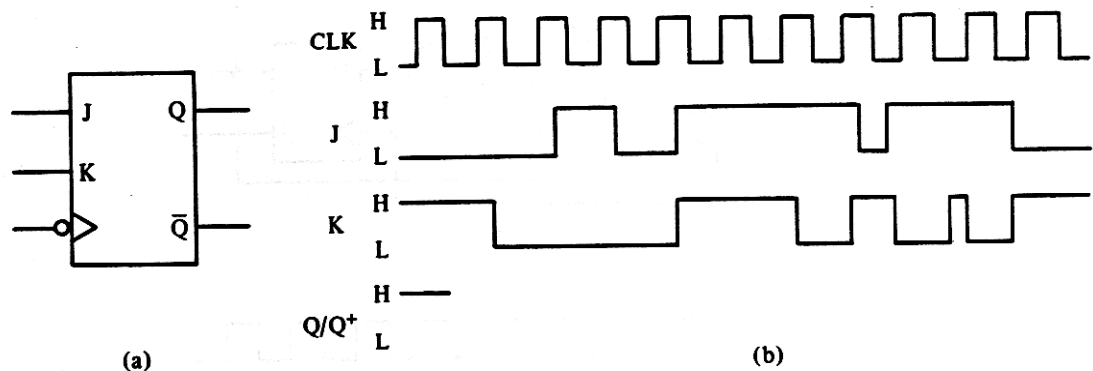


(a)

(b)

Figure 5.29 Circuit diagram and timing diagram for Problem 5.3.

5.4. Figure 5.30(a) shows a J-K flip-flop with an active-low clock input.



(a)

(b)

Figure 5.30 J-K flip-flop and timing diagram for Problem 5.4.

(a) Complete the timing diagram of Fig. 5.30(b) and compare it with the one shown in Fig. 5.2(c). Show the propagation delays  $t_{pHL}$  and  $t_{pLH}$ .

(b) Redraw the timing diagram without showing the propagation delays.

5.5. Recall that binary subtraction can be performed by adding the 2s-complement form of the subtrahend to the minuend. In other words,

$$A - B = A + (-B)$$

With this in mind, convert the serial adder shown in Fig. 5.5(a) into a serial subtractor. What must be the initial value of the D flip-flop output? Assume that a 74'74 D flip-flop, as shown in Fig. 5.6(a), is to be used. Be sure to initialize the contents of the D flip-flop with an active-low signal, INIT\_PULSE ( ).

5.6. Convert the serial adder of Fig. 5.5(a) into a serial adder/subtractor, the block diagram of which is shown in Fig. 5.31. The operation is as follows: When  $\bar{A}/S$  is false (L), the addition operation is performed. But when  $\bar{A}/S$  is true (H), the subtraction operation is performed. The active-low signal INIT\_PULSE is used to initialize the D flip-flop contents. Assume that a 74'74 D flip-flop is to be used. (Hint: Also use an XOR gate and an inverter.)

*(Hint: An XOR gate would be useful.)*

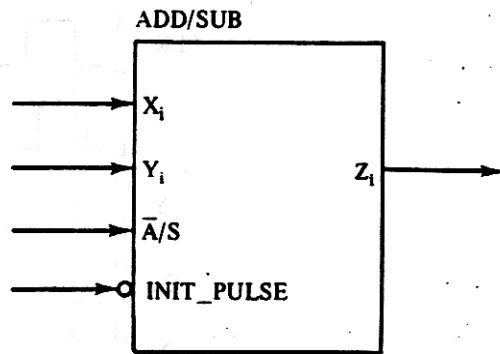


Figure 5.31 Serial adder/subtractor for Problem 5.6.

- 5.7. (a) Analyze the circuit diagram of Fig. 5.32(a) and complete the timing diagram of Fig. 5.32(b). Do not show the propagation delays.  
 (b) Assuming that the circuit of Fig. 5.32(a) represents a type of flip-flop, derive its characteristic table and its condensed characteristic table.  
 (c) Derive its excitation table.

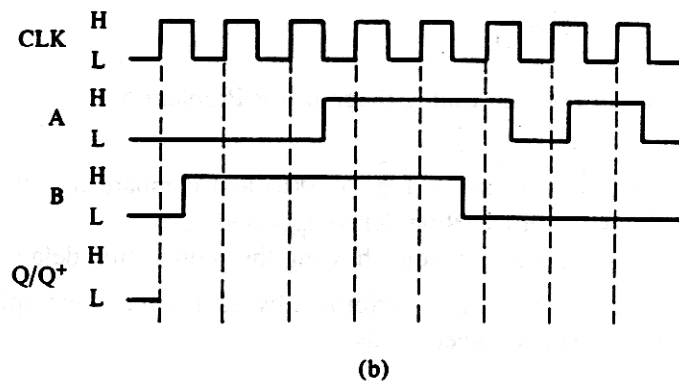
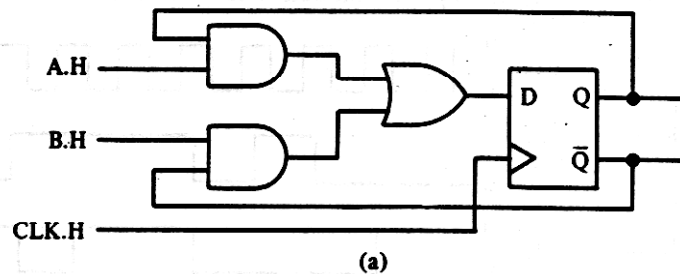
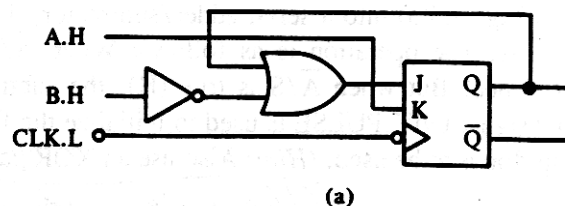
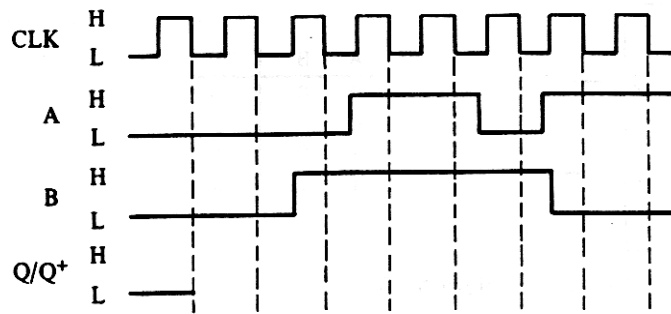


Figure 5.32 Circuit and timing diagrams for Problem 5.7.

- 5.8. Repeat Problem 5.7 for the circuit and timing diagrams of Fig. 5.33. Note that the clock input is active-low.





(b)

Figure 5.33 Circuit and timing diagrams for Problem 5.8.

- 5.9. Implement a J-K flip-flop using a 74'74 D flip-flop and any gates that are needed. Label all gates.
- 5.10. Implement a T flip-flop using a 74'74 D flip-flop and any gates that are needed. Label all gates.
- 5.11. Implement the unclocked  $S^*-R^*$  flip-flop of Fig. 5.34 with a normal unclocked S-R flip-flop and any gates that are needed. An unclocked  $S^*-R^*$  flip-flop functions exactly like a normal unclocked S-R flip-flop except that  $S^* = R^* = 1$  is allowed. For this input the  $S^*-R^*$  flip-flop retains its previous Q value.

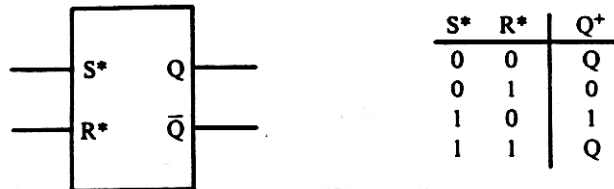


Figure 5.34 Flip-flop for Problem 5.11.

- 5.12. The A-B flip-flop of Fig. 5.35 is to be implemented. Note that this flip-flop functions as a J-K flip-flop except for the inputs  $A = B = 1$ , for which the "set" input A dominates.

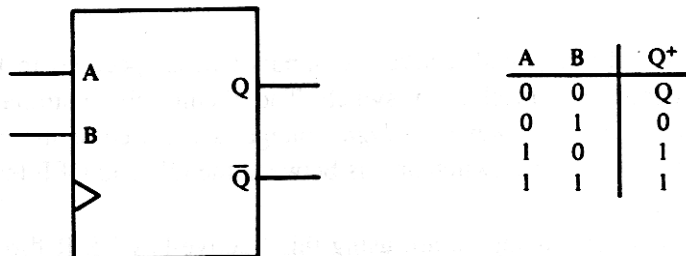


Figure 5.35 Flip-flop for Problem 5.12.

- (a) Implement it using a 74'109 J-K flip-flop plus any gates that are needed.
- (b) Implement it using a 74'74 D flip-flop plus any gates that are needed.
- (c) Implement it using the T flip-flop of Fig. 5.7 plus any gates that are needed.

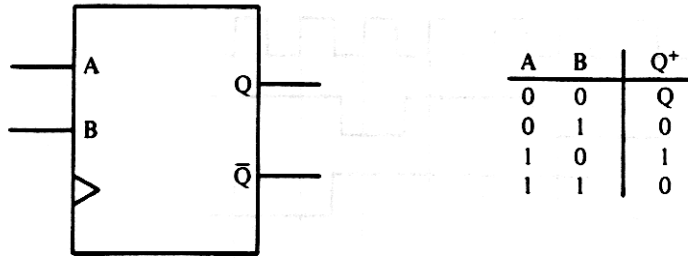


Figure 5.36 Flip-flop for Problem 5.13.

- 5.13. Repeat Problem 5.12 for the A-B flip-flop of Fig. 5.36. Note that this flip-flop functions as a J-K flip-flop except for the inputs  $A = B = 1$ , for which the "clear" input B dominates.
- 5.14. (a) Given the truth table of Fig. 5.11(b) for an unclocked S-R flip-flop, determine the logic equation for  $Q^+$  as a function of S, R, and Q.  
 (b) The circuit diagram of Fig. 5.13(a) is the most popular gate implementation for an S-R flip-flop. Algebraically show that this implementation is consistent with your answer to part (a).  
 (c) Draw a mixed-logic circuit diagram corresponding to your answer to part (a).
- 5.15. Using commercially available gates, implement the unclocked S-R flip-flop of Fig. 5.37. Note the active-low inputs. Specify and label all components and signals.

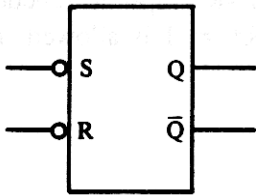


Figure 5.37 S-R flip-flop for Problem 5.15.

- 5.16. The operation of the switch debouncing circuit of Fig. 5.12(c) depends upon the voltage levels at the S and R inputs being both L when the switch arm is not in contact with either the ON or OFF terminal. For this L voltage level to occur, the resistor resistances must be small enough that the voltages at the S and R inputs are less than or equal to  $V_{IL}$ , which is 0.8 V for LS-TTL. With this in mind, determine the maximum resistance,  $R_{max}$ , allowable for the resistors. Use LS-TTL values.
- 5.17. The unclocked S-R flip-flop with active-low inputs that is specified in Problem 5.15 can also be used to debounce a mechanical switch. The circuit will be similar to that shown in Fig. 5.12(c). In this case, however, a *high* voltage is required at the S and R inputs to present a false value when the switch arm is between the ON and OFF terminals. With this in mind,  
 (a) Design a switch debouncing circuit using this "active-low" S-R flip-flop.  
 (b) Determine the minimum resistance,  $R_{min}$ , of the resistors that will give proper operation when the switch arm is between the ON and OFF terminals. Use LS-TTL values.
- 5.18. Complete the timing diagram of Fig. 5.38, which is for the unclocked J-K flip-flop shown in Fig. 5.14. Show the propagation delays  $t_{pHL}$  and  $t_{pLH}$ . Also, what happens after  $t_f$ ?

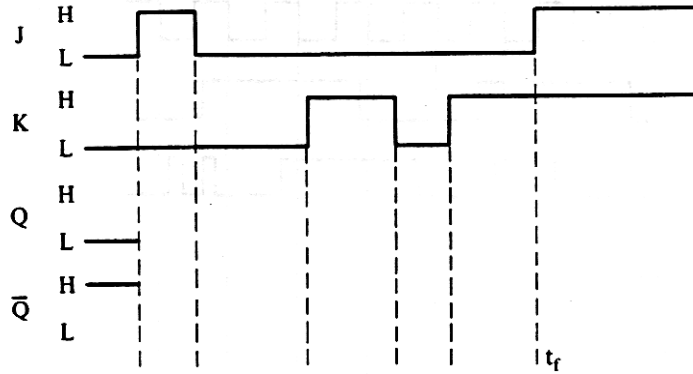


Figure 5.38 Timing diagram for Problem 5.18.

- 5.19. The circuit diagram of Fig. 5.15 is for a clocked J-K flip-flop.
- How does this flip-flop differ from the clocked J-K flip-flop discussed in Sec. 5.3.1?
  - What is the restriction on the clock signal for the flip-flop shown in Fig. 5.15? Why?
- 5.20. Complete the timing diagram of Fig. 5.39 for the 74'107 J-K flip-flop of Fig. 5.3(a) to demonstrate the difference between a synchronous and an asynchronous clear operation. Do not show the propagation delays.

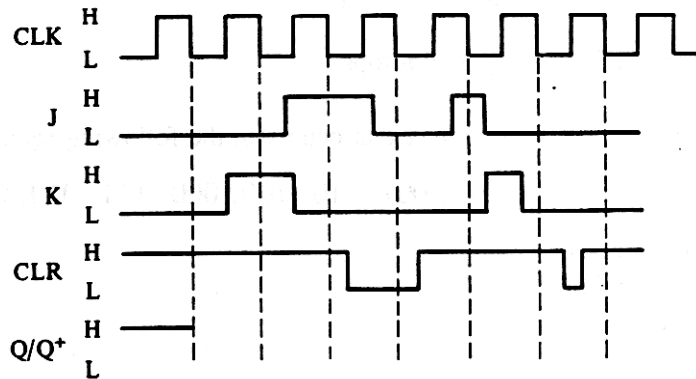
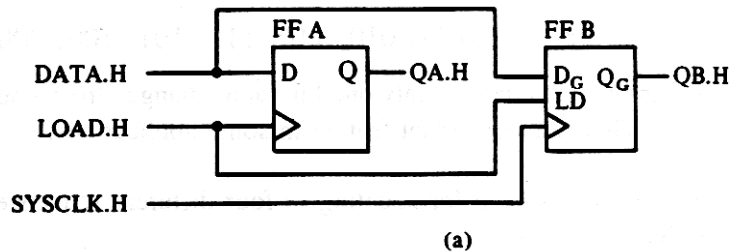
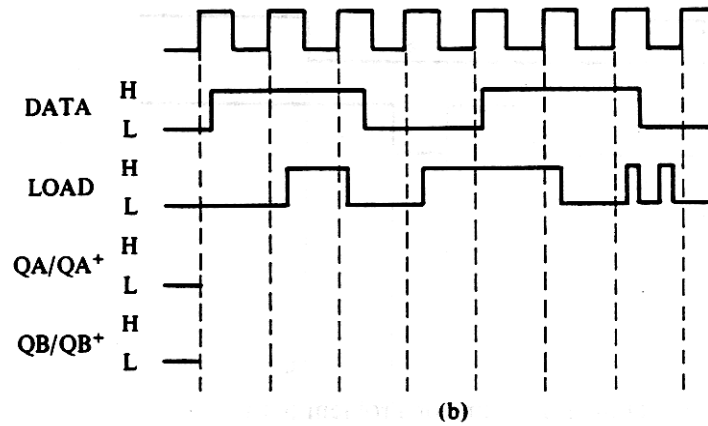


Figure 5.39 Timing diagram for Problem 5.20.

- 5.21. Given the circuit diagram of Fig. 5.40(a) consisting of a normal D flip-flop and a gated D flip-flop (see Example 5.2 and Fig. 5.8 for details), complete the timing diagram of Fig. 5.40(b). Do not show the propagation delays.





**Figure 5.40** Circuit diagram and timing diagram for Problem 5.21.

- 5.22.** A 4-bit binary counter is to be designed and realized using D flip-flops. The count is to be as follows:

. . . , 0000, 0001, 0010, 0011, 0100, . . . , 1110, 1111, 0000, 0001, . . .

- (a) Draw the state diagram for the count sequence.
- (b) Draw the functional block diagram for the counter, including the D flip-flops and the corresponding combinational circuit, in the manner shown in Fig. 5.18(a).
- (c) Determine the required logic equations and draw the circuit diagram for the counter.

- 5.23.** Repeat Problem 5.22 using J-K flip-flops.

- 5.24.** Repeat Problem 5.22 using T flip-flops.

- 5.25.** Design and realize a 3-bit counter that counts in the following sequence:

. . . , 111, 010, 001, 110, 100, 000, 111, 010, 001, . . .

- (a) Use D flip-flops.
- (b) Use J-K flip-flops.
- (c) Use T flip-flops.

- 5.26.** Design and realize a 4-bit decade counter with a synchronous CLEAR input. Use D flip-flops.

- 5.27.** Design and realize a 3-bit Gray-code counter with an enable (EN) input. Use J-K flip-flops. The counter is to count in the prescribed Gray-code sequence if EN is true at the next active clock transition. But if EN is false at this transition, then the counter does not count and, instead, retains its current value. The Gray-code sequence is as follows:

. . . , 000, 001, 011, 010, 110, 111, 101, 100, 000, 001, . . .

Observe for the Gray code that only one bit value changes from one number to the next in the sequence. This is an important feature in some applications.

- 5.28.** A counter is to be designed for counting in four different sequences under the control of two inputs  $X_1$  and  $X_2$  as follows:



- 5.31. Show that the 4-bit binary down-counter of Fig. 5.43 can be realized with only a 74'163. No additional components are needed.

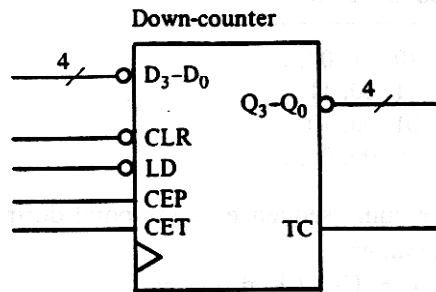


Figure 5.43 Down-counter for Problem 5.31.

- 5.32. Using a 74'163 and any gates that are needed, realize a decade counter similar to the 74'162.
- 5.33. Design and implement the counter circuit of Fig. 5.44 using a 74'163 and any gates that are needed. This circuit is to be used to determine if an event has occurred ten or more times. It is synchronously cleared when the CLR input is equal to true or when the count has reached 1111. This counter circuit will count only if it detects a true value at the EVENT input at an active clock transition. The (COUNT  $\geq$  10) output is true only when the count is greater than or equal to 1001.

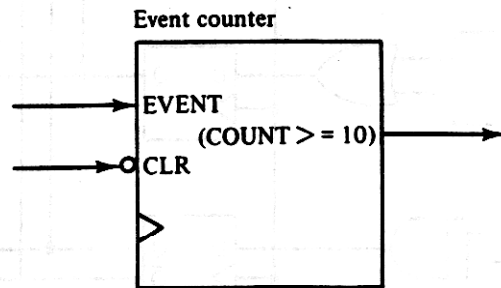
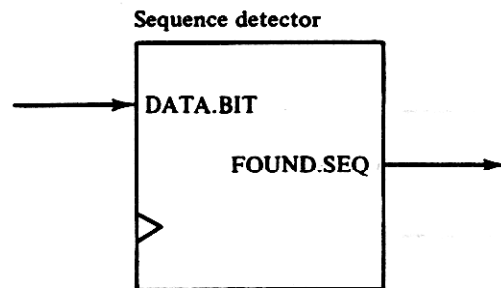


Figure 5.44 Counter circuit for Problem 5.33.

- 5.34. Show what must be done to the 74'194 to transform it into a 4-bit storage register.
- 5.35. Using a 74'194 and any gates that are needed, design and implement the sequence detector circuit shown in Fig. 5.45(a). The circuit input is a sequence of 1-bit values (either a 0 or a 1) detected at each active transition of the clock signal. When the circuit detects the sequence 1101, the output FOUND.SEQ becomes true for one clock cycle, as shown in the timing diagram of Fig. 5.45(b).



(a)