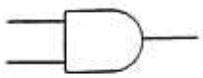
A	B	C	Z
F	F	F	F
F	F	T	T
F	T	F	T
F	T	T	F
T	F	F	T
T	F	T	F
T	T	F	T
T	T	T	T

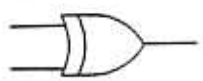
3.8. (a) Show how a 74'00 gate can be made into an inverter.
(b) Is it a logic inverter or a voltage inverter? Explain.

3.9. (a) By looking into a TTL data book, find the 74'Y component corresponding to the following logic symbol:



(b) Determine the voltage table for it.
(c) List the eight possible logic/voltage assignments.
(d) For each of the eight assignments, determine (using the voltage and logic tables) the logic function that this component performs.
(e) What logic function does it perform for the positive-logic convention?
(f) What logic function does it perform for the negative-logic convention?

3.10. Repeat Problem 3.9 for the following logic symbol:



3.11. Find voltage tables for the devices of Fig. 3.23.

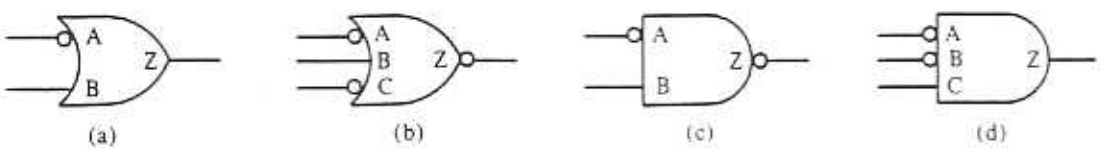


Figure 3.23 Devices for Problem 3.11.

3.12. Find the logic expressions for the Z outputs in Fig. 3.24.

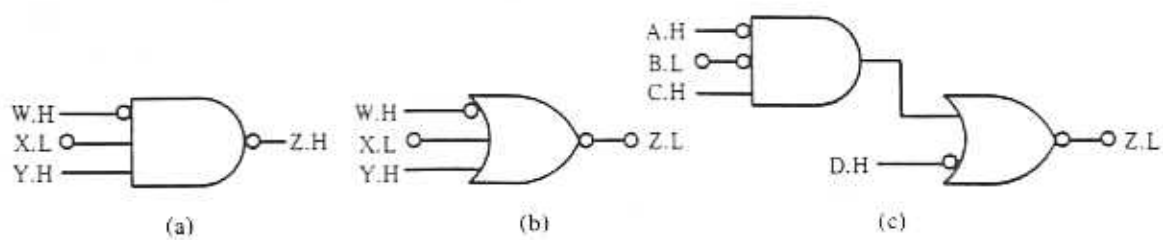


Figure 3.24 Devices for Problem 3.12.

3.13. Fill in all the intermediate signal names for the mixed-logic circuit diagram of Fig. 3.25. Also, find a logic expression for Z.

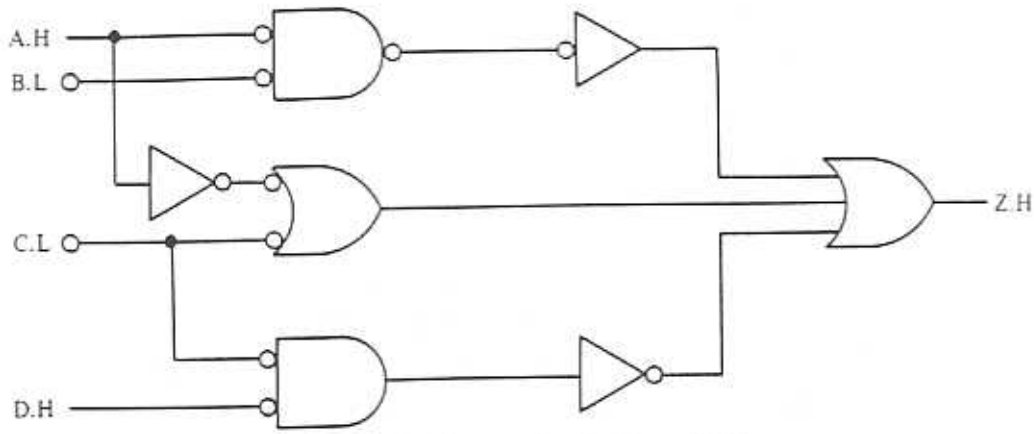


Figure 3.25 Mixed-logic circuit diagram for Problem 3.13.

3.14. Repeat Problem 3.13 for the circuit diagram of Fig. 3.26.

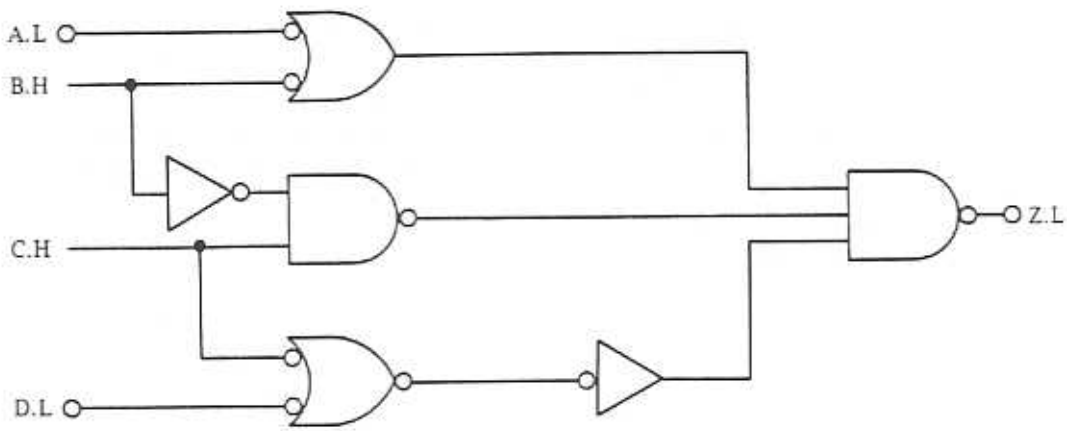


Figure 3.26 Mixed-logic circuit diagram for Problem 3.14.

3.15. Repeat Problem 3.13 for the circuit diagram of Fig. 3.27.

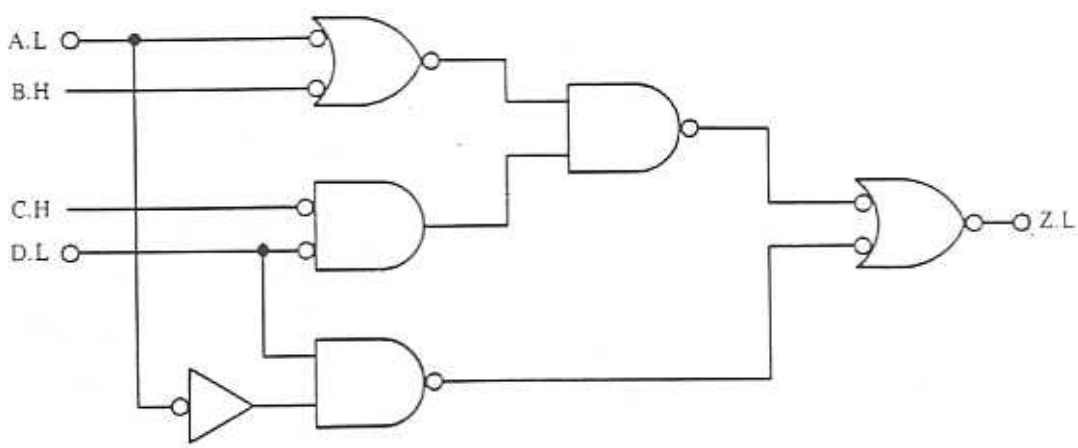


Figure 3.27 Mixed-logic circuit diagram for Problem 3.15.

3.16. Figure 3.28 shows a circuit based on the positive-logic convention. Fill in all the intermediate signal names and find a logic expression for Z. Compare with the answer to Problem 3.13.

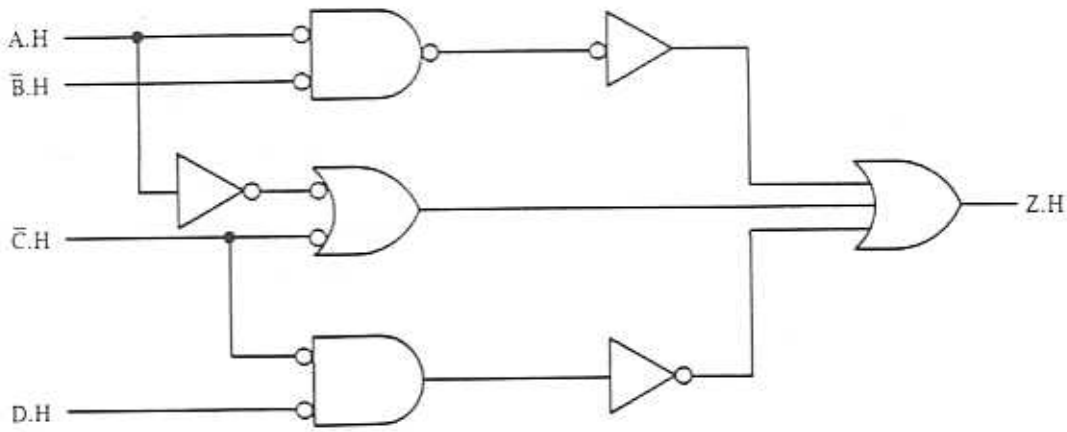


Figure 3.28 Positive-logic circuit diagram for Problem 3.16.

3.17. Repeat Problem 3.16 for the circuit of Fig. 3.29. Compare with the answer to Problem 3.14.

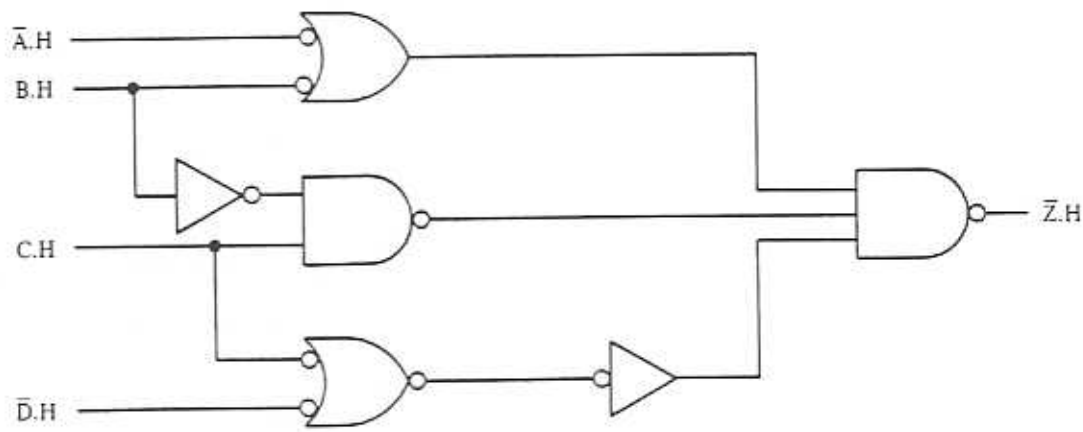


Figure 3.29 Positive-logic circuit diagram for Problem 3.17.

3.18. Repeat Problem 3.16 for the circuit of Fig. 3.30. Compare with the answer to Problem 3.15.

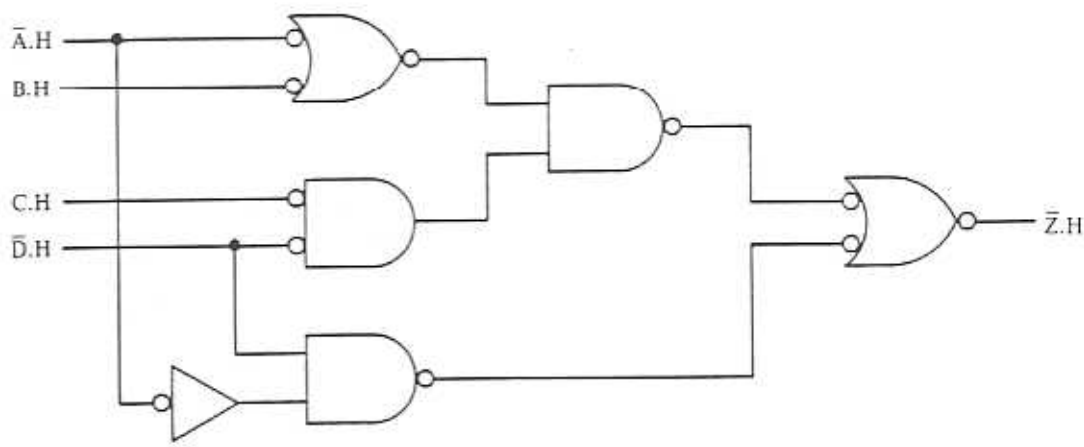


Figure 3.30 Positive-logic circuit diagram for Problem 3.18.

3.19. Analyze each circuit diagram of Fig. 3.31 and determine the logic equation for Z based on the positive-logic convention. Remember that in the positive-logic convention, all inverters and inverting circles perform a logic inversion.

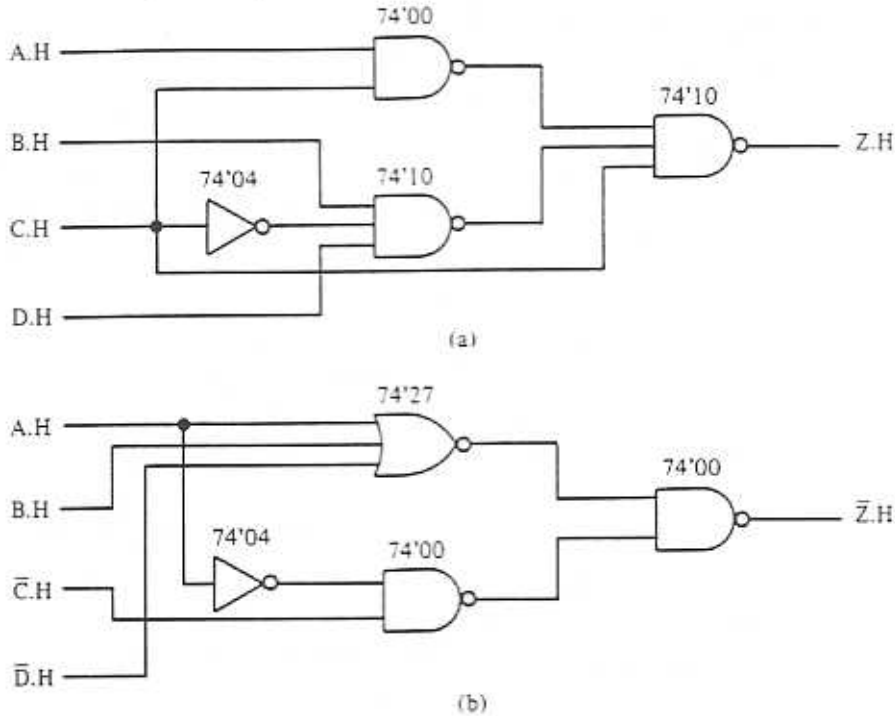


Figure 3.31 Circuit diagrams for Problem 3.19.

3.20. Analyze each circuit diagram of Fig. 3.32 and determine the logic equation for Z based on the mixed-logic convention. Remember that in the mixed-logic convention, a logic NOT occurs as a result of a "mismatched" logic/voltage assignment.

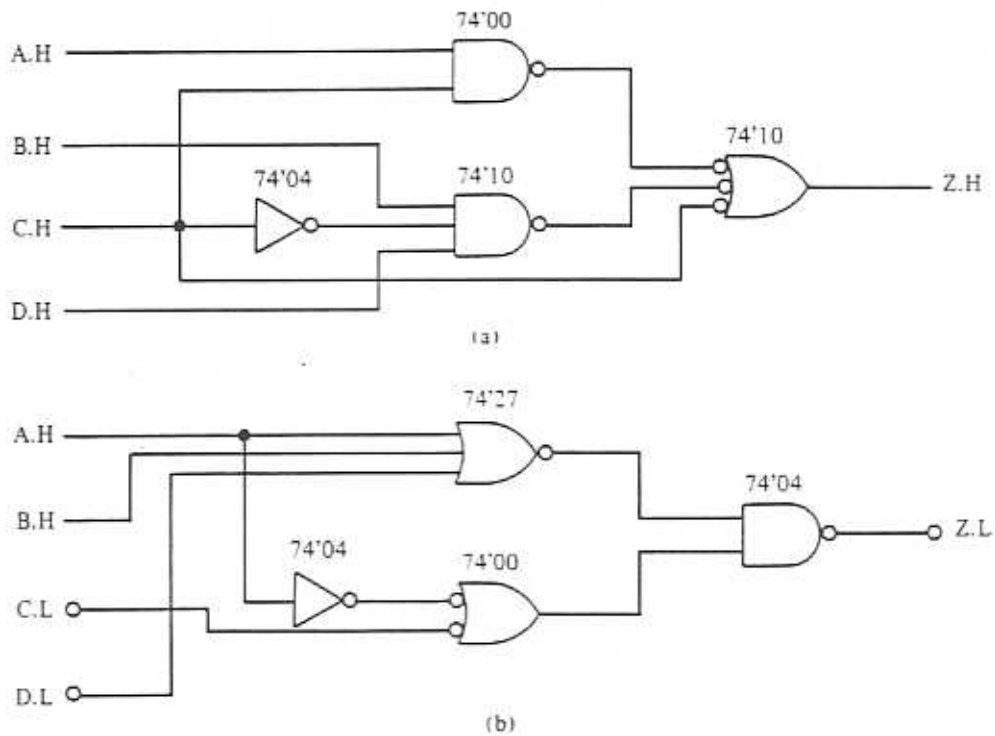


Figure 3.32 Circuit diagrams for Problem 3.20.

3.21. Figure 3.33 shows a two-level NAND logic diagram based on the positive-logic convention. (The number of levels is the maximum number of gates that signals must pass through.) Find an SOP expression for Z.

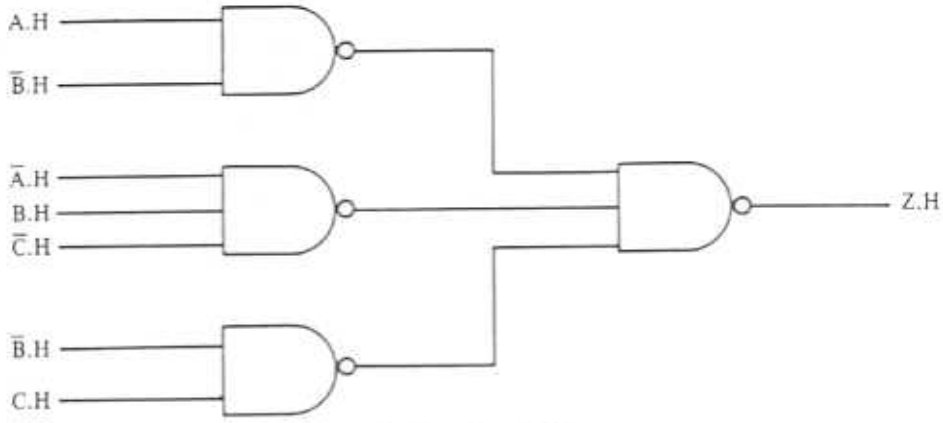


Figure 3.33 Logic diagram for Problem 3.21.

3.22. Implement each of the following using an optimum two-level positive-logic NAND realization. In other words, only NAND gates are available for the implementation, and they are to be used in no more than two levels. Assume that the variables and their complements are both available for inputs.

(a) $Z = \overline{A}\overline{B} + \overline{B}C$

(b) $Z = (\overline{A} + B + \overline{C})(\overline{B} + C)$

(c) $Z = \overline{A}CD + AC\overline{D} + AB + B\overline{C}\,\overline{D}$

(d) $Z = (B + \overline{D})(A + \overline{B})(\overline{B} + C + D)$

3.23. Figure 3.34 shows a two-level NOR logic diagram based on the positive-logic convention. Find a POS expression for Z.

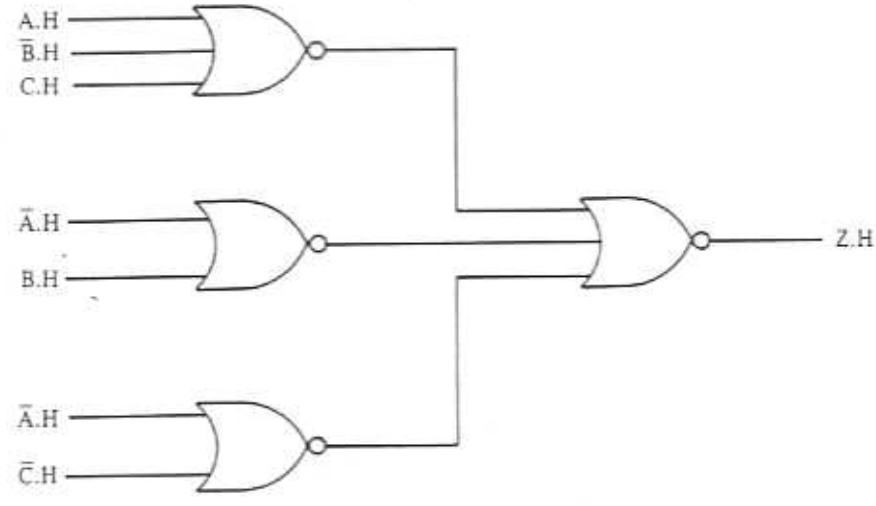


Figure 3.34 Logic diagram for Problem 3.23.

3.24. Implement each of the following using an optimum two-level positive-logic NOR realization. In other words, only NOR gates are available for the implementation, and they are to be used in no more than two levels. Assume that the variables and their complements are both available for inputs.

(a) $Z = (\overline{A} + \overline{B})(\overline{B} + C)$

(b) $Z = A\overline{B}\,\overline{C} + \overline{A}C$

(c) $Z = (\overline{A} + C + D)(A + C + \overline{D})(A + B)(B + \overline{C} + \overline{D})$

(d) $Z = B\overline{D} + A\overline{B} + \overline{B}CD$

3.25. Implement the following logic equations for Z, basing the implementations on the positive-logic convention. Assume that only the following gates are available: 74'00, 74'02, 74'04, 74'10, and 74'27. Also, for each implementation use a minimum number of gates and draw the circuit diagram with all gates labeled.

(a) $Z = AB + \overline{C} + \overline{A}\,\overline{B}\,\overline{D}$ for Z.H. The inputs are A.H, B.H, C.H, and D.L.

(b) $Z = (A + D)(\overline{A} + C + \overline{D})(\overline{C} + D)$ for Z.H. The inputs are A.H, B.L, C.H, and D.H.

(c) $Z = \overline{A\overline{B}} + \overline{C}D + C\overline{D}$ for Z.H. The inputs are A.L, B.H, C.H, and D.L.

(d) $Z = \overline{(A + \overline{D})(\overline{B} + C)(B + \overline{C})}$ for Z.H. The inputs are A.H, B.L, C.H, D.H, and D.L.

(e) $Z = \overline{A\overline{C}} + BD + \overline{B}\,\overline{D}$ for Z.L. The inputs are A.L, B.L, C.H, and D.H.

(f) $Z = A\overline{C} + BD + C\overline{D}$ for Z.L. The inputs are A.L, B.L, C.H, and D.L.

3.26. Repeat Problem 3.25 for implementations based on the mixed-logic convention.

3.27. Implement the following logic equations for Z, basing the implementations on the positive-logic convention. Draw the circuit diagrams with all gates labeled. Select any gates from a TTL data book, and the 74'86 Exclusive OR gate in particular. But, minimize the number of *IC packages* used. In other words, try to use the same types of gates when possible.

(a) $Z = AB + \overline{A \odot C} + \overline{A}C$ for Z.L. The inputs are A.H, A.L, B.L, C.H, and C.L.

(b) $Z = \overline{A \oplus B} + \overline{B} \odot C + \overline{\overline{C}D}$ for Z.H. The inputs are A.H, B.H, C.L, and D.H.

(c) $Z = A\overline{B} + B \oplus D$ for Z.H. The inputs are A.H, B.L, C.L, and D.H.

3.28. Repeat Problem 3.27 for the mixed-logic convention.

3.29. Figure 3.35 shows a parity detector for detecting the parity of an input 4-bit number ABCD. The detector output PARITY is 0 (PARITY = 0) if ABCD has even parity, which means that ABCD contains an even number of 1s. And the output PARITY is 1 (PARITY = 1) if ABCD has odd parity, which means that it contains an odd number of 1s. For example, for ABCD = 0110, PARITY = 0. And for ABCD = 1101, PARITY = 1.

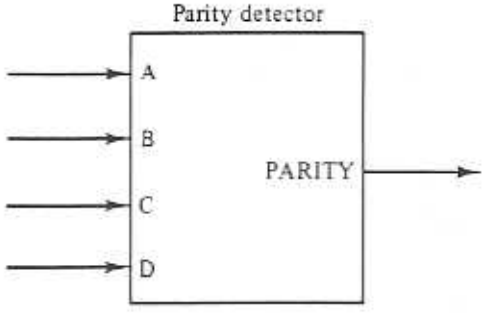


Figure 3.35 Parity detector for Problem 3.29.

(a) Make a truth table for the parity detector, with input columns of ABCD and an output column of PARITY.

(b) Determine an MSOP expression for PARITY.

(c) For inputs of A.H, B.H, C.H, and D.H, implement the MSOP logic equation for PARITY.H using the positive-logic convention.

(d) Repeat part (c) for the mixed-logic convention.

3.30. A combinational circuit with inputs A, B, C, and D and an output Z is to be designed such that Z = 1 if and only if three or more of the inputs are 1.

(a) Make a truth table for the circuit.

(b) Determine an MSOP expression for Z.

(c) For inputs of A.H, B.H, C.H, and D.H, implement the MSOP logic equation for Z.H using the positive-logic convention.

(d) Repeat part (c) for the mixed-logic convention.

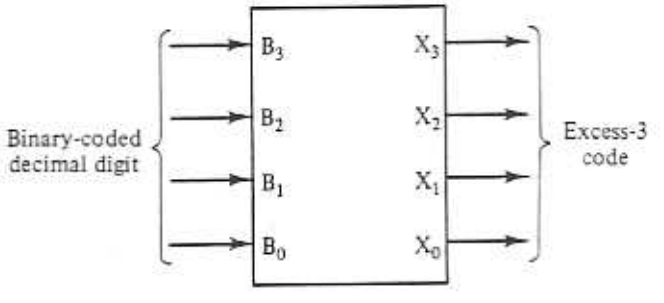
3.31. Figure 3.36 shows an excess-3 code generator and table. An excess-3 code is a binary code for decimal numbers in which each *decimal digit* is represented by its binary equivalent *plus 3*. For example, the excess-3 code for the digit 0 is 0011, and for the digit 9 it is 1100. A characteristic of the excess-3 code is that every coded digit has at least one 1, which is important in some applications.

(a) Complete the truth table for the circuit, using don't cares for invalid inputs.

(b) Determine MSOP expressions for the four outputs X_3, X_2, X_1, and X_0.

(c) Implement the MSOP logic equations for the four outputs, basing the implementations on the positive-logic convention. Assume that all inputs and outputs are active-high.

(d) Repeat part (c) for the mixed-logic convention, again assuming that all inputs and outputs are active-high.



B_3	B_2	B_1	B_0	X_3	X_2	X_1	X_0
0	0	0	0	0	0	1	1
0	0	0	1				
		⋮				⋮	
1	0	0	1	1	1	0	0
1	0	1	0				
		⋮				⋮	
1	1	1	1				

Figure 3.36 Excess-3 code generator and table for Problem 3.31.

3.32. A large room has three entrances, each with a light switch that controls an overhead light. A combinational circuit is to be designed with inputs A, B, and C from the individual light switches and an output LIGHT for controlling the energization of the overhead light. When all three switches are down (i.e., A = 0, B = 0, and C = 0), then the light is to be off (LIGHT = 0). Also, a change in position of any switch will change the state of the light. Assume that only one switch can be changed at a time.

(a) Draw a block diagram of this circuit

(b) Make a truth table for the circuit.

(c) Determine an MSOP expression for LIGHT.

(d) Implement the MSOP logic equation for $\overline{\text{LIGHT}}$.H, basing the implementation on the positive-logic convention. Assume that the inputs are active-high.

(e) Repeat part (d) for the mixed-logic convention, again assuming that all inputs are active-high.

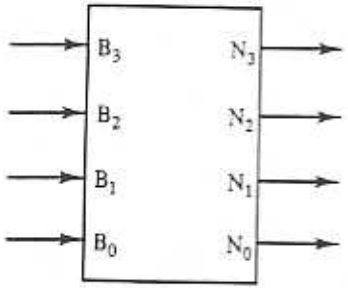
3.33. The input to the combinational circuit of Fig. 3.37 is a 4-bit binary number $B_3B_2B_1B_0$. The function of this circuit is to convert this binary number into the corresponding negative number $N_3N_2N_1N_0$ in 2s-complement form.

(a) Complete the truth table for the circuit.

(b) Determine MSOP expressions for the four outputs N_3, N_2, N_1, and N_0.

(c) Implement the MSOP logic equations for the four outputs, basing the implementations on the positive-logic convention. Assume that all inputs and outputs are active-high.

(d) Repeat part (c) for the mixed-logic convention, again assuming that all inputs and outputs are active-high.



B_3	B_2	B_1	B_0	N_3	N_2	N_1	N_0
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
⋮						⋮	
1	1	1	1	0	0	0	1

Figure 3.37 Combinational circuit and table for Problem 3.33.

3.34. What are the advantages and disadvantages of synthesis based on the positive-logic convention?

3.35. What are the advantages and disadvantages of synthesis based on the mixed-logic convention?