HOMEWORK 10

Revision **0**

*Note: Late HW is **not** accepted!*

From the Lam book problems:

7.3, 7.5, 7.8, 7.15, 7.18

7.19 => convert to an ASM chart
=> implement the system using a ROM and JK flip-flops only
=> with X1.H, X2.L, Z1.H, Z2.L, Z3.H

7.23

Redo your Lab 2 combinatorial circuits **for the Hex to 7-Segment Decoder**, replacing the ANDs, ORs, NOTs, etc. with VHDL code. (See the *Creating graphical components* file on the website for information on how to incorporate VHDL code in a bdf file. This file can be found on the Software/Docs webpage, adjacent to the Quartus heading.)

a) Include a screenshot of your VHDL file **in your pdf** submission. Be sure to put your name, the HW number, the due date and the description of what the file is supposed to do in the comments section at the beginning of the VHDL file.
b) Make a component with your VHDL file, replace your Lab 2 combinatorial elements, and adequately simulate the entire design. Also include a screenshot of both the bdf and the simulation in your pdf submission.