HOMEWORK 4

Revision **0**

*Note: Late HW is **not** accepted!*

In this course (in homework, labs, exams, etc.), for all mixed-logic circuit diagrams, write the intermediate equations at the inputs of <u>each</u> gate.

1. Do the following **Roth** textbook problems:

   5th edition:
   - 2.1a, 2.1c, 2.3a, 2.3d, ~~2.4b,~~ 2.7a, 2.13a
   - 3.6b, 3.9, ~~3.14a,~~ ~~3.18b,~~ 3.27 ~~a, b, c,~~ d
   - 4.1a, ~~4.1b,~~ 4.6a, 4.7a

   6th edition:
   - 2.1a, 2.1c, 2.3a, 2.3d, ~~2.4b,~~ 2.7a, 2.13a
   - 3.6b, 3.9, ~~3.15a,~~ ~~3.21b,~~ 3.32 ~~a, b, c,~~ d
   - 4.1a, ~~4.1b,~~ 4.6 a, 4.7a

   7th edition:
   - 2.1a, 2.1c, 2.3a, 2.3d, ~~2.4b,~~ 2.7a, 2.13a
   - 3.6b, 3.9, ~~3.15a,~~ ~~3.21b,~~ 3.32 ~~a, b, c,~~ d
   - 4.1a, ~~4.1b,~~ 4.6 a, 4.7a

2. Prove that:
   a) X xor 0 = X
   b) X xor 1 = /X

3. **Lam/O'Malley/Arroyo** textbook problems: (Get these problems from the class web site.)
   In this textbook, it should be noted that a bubble shown at an input is a redundant notation that indicates that a signal is active-low. This bubble does **NOT** do anything else.

   3.13, 3.20,
   3.26 ~~a, c,~~ e (do not attempt to simplify)