I. From Mano textbook, do the following problems:
   Chapter 2: problem 2.6 (b, d, e)
   Chapter 2: problem 2.24 (a, b, c); **BUT, DO THE FOLLOWING:** For each of the three parts (a, b, and c), determine the K-map. Then, determine the MSOP expression **AND** the MPOS expression.
   Chapter 2: problem 2-26(a).

II. Implement the following logic equations for Z. Implement them as they are. Do not transform or minimize the equations. Assume that only the following gates are available: 74'00, 74'02, 74'04, 74'10, and 74'27. For each implementation, use a minimum number of gates and draw the circuit diagram with all gates labeled (e.g., 74'00 or 74’10, etc.).
   (a) \( Z = AB + /C + /A/B/D \) for Z.H. The inputs are A.H, B.H, C.H, and D.L.
   (b) \( Z = (A + D) (/A + C + /D) (/C + D) \) for Z.H. The inputs are A.H, B.L, C.H, and D.H.
   (c) \( Z = /(A/B) + /CD + C/D \) for Z.H. The inputs are A.L, B.H, C.H, and D.L.

III. Analyze the following circuit and find a logic expression for Z. Also, fill in all the intermediate signal names.
   (a)
IV. Implement the following logic equations for Z. Implement them as they are. Do not transform or minimize the equations. Assume that only the following gates are available: 74’00, 74’02, 74’04, 74’10, and 74’27. For each implementation, use a minimum number of gates and draw the circuit diagram with all gates labeled (e.g., 74’00 or 74’10, etc.).

(a) \( Z = \overline{A/C} + BD + \overline{B/D} \) for Z.L. The inputs are A.L, B.L, C.H, and D.H.
(b) \( Z = A/C + BD + C/D \) for Z.L. The inputs are A.L, B.L, C.H, and D.L.