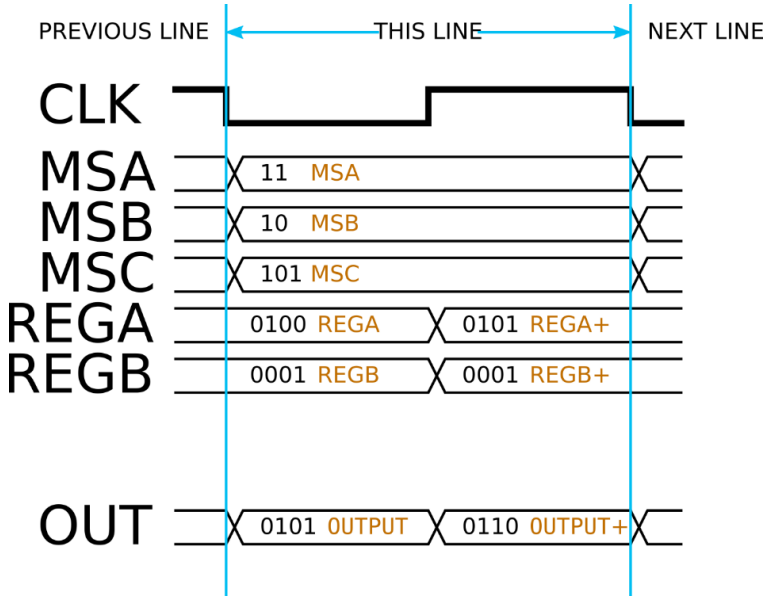
In the past, some students have had trouble with the table at the end of the Lab 4 document. Let's take a closer look at what a line in this table means:

MSA	MSB	MSC	INPUT	Cin	REGA	REGB	OUTPUT	REGA+	REGB+	OUTPUT+	Description
11	10	100	XXXX	0	0100	0001	0101	0101	0001	0110	REGA ← REGA + REGB

This line adds REGA to REGB and stores the result in REGA. But how does it do that? Let's look at a simulation, to see how it translates into actual signal values:



The first thing to notice is that this line's "section" of the simulation starts on the falling edge. The start of a table line occurs when you change the MSA/B/C and the input values. This does not necessarily have to be on the falling-edge of the clock; however, it should never be on the rising-edge. In a simulation, this is done to avoid ambiguity regarding whether the flip-flop outputs or the input signals change first. In a practical circuit, changing inputs on the rising clock-edge could cause a flip-flop to enter an unpredictable, “metastable state,” where the output is neither high nor low.

Now, look at OUTPUT. Notice how it changes as soon as the inputs change (actually, a propagation delay later, which we would see if we had a timing simulation), becoming the result of adding REGA and REGB. OUTPUT is **not** a register, so it will not remember the value it held in any previous line of the table. It is always a function of REGA, REGB, Cin, and MSC; it does not depend on anything else. MSC changes at the start of the line, so OUTPUT changes in response.

When the rising-edge occurs, REGA and REGB change. The new result is based on MSA/B and the buses leading into them; REGA+ and REGB+ are simply the new values that REGA and REGB hold after the clock-edge. They will always be the same as the next line's REGA and REGB, since they only change on the rising-edge.

Notice that OUTPUT also changes. This is because REGA/REGB changed. We have not changed MSC yet; that won't happen until the next cycle starts. So the new value (which is labeled OUTPUT+ on the table) is just the result of taking the current line's operation (in this case, the sum of REGA, REGB, and Cin) and applying it to REGA+ or REGB+. Unlike REGA+ and REGB+, OUTPUT+ will **not** persist into the next cycle; as soon as MSC changes, the output value will change to reflect the new operation. Thus, it will not necessarily be the same as the OUTPUT value from the previous line.

Of course, OUTPUT will sometimes be the same as OUTPUT+, and one line's OUTPUT+ will sometimes be the same as the next line's OUTPUT. This depends on whether REGA/REGB/MSC change on a given clock-edge or between two lines in the program.