LAB 2: Logic Design

OBJECTIVES:

- To understand the operation of Quartus as a digital design and simulation tool.
- To learn how to realize a digital design with discrete components (IC’s, LED’s, switches, and resistors).
- **Note:** Do not use the 74* objects of Quartus in the other maxplus2 library when constructing a design with basic logic gates in this course. Instead use gates such as AND, NOR, NOT, etc., in the primitives | logic library. You must add the pin numbers and label each gate with the chip number (e.g., ’02 when using a 74HC02) for all designs that you will construct.

MATERIALS:

- Hardware (Protoboard, ICs, LED’s, multimeter, etc.) you received during Lab 1. Unless otherwise stated, design only with parts that you have in your kits.
- Layout file (protoboard_for_layout) on our web site
- Your own laptop computer.
- Printouts required for this and every lab: this lab document, a Pinouts document, the Quartus tutorial, the Hardware: Getting Started document, the pre-lab designs and simulations. All designs and simulations done in pre-lab must be printed and brought to lab. All simulations should be annotated (using Quartus) to highlight key points in the simulation. All Quartus schematic printouts throughout the semester should include your name, printed using Quartus and using a 20pt font. All pre-lab material is turned in at the beginning of lab. You will not get this paperwork back until the following lab. Since you are likely to need this material during lab, we suggest that you make a second copy for yourself before coming to lab. It is much easier to debug a circuit from paper then from a laptop screen.

INTRODUCTION

You should be familiar with the operation of the Quartus software, the breadboard functions, and basic logic design prior to arriving at the laboratory.

TOTAALLY OPTIONAL PRE-PRE-LAB

This section is for your eyes only, i.e., it will not be turned in; it will help you understand the big picture.

Do all that is described in the pre-lab below, but use a simpler equation, e.g. \( W = (A \cdot B) \).

PRE-LAB REQUIREMENTS

1. Using only AND gates with NO bubbles, OR with NO bubbles, and NOT gates, design and draw the circuit for the following logic equation. \( V = [ (A \cdot B) + (C + /D) ] \) 

2. Most of the world uses positive-logic only; and so will you in this section (and in the previous section). Draw the circuit for the equation below by hand and then with Quartus using only the positive-logic gates (i.e., AND, OR, NAND, NOR, and NOT gates) and active-high inputs and output. (Positive-logic gates do not have bubbles at input pins.)

   \[
   W = [ (A \cdot B) + (C + /D) ]
   \]

   Note that this equation has the same right-hand side as the equation (1). Do not simplify or otherwise manipulate the equation, i.e., do not use BAND2 instead of NOR2 even when you want an AND function.

3. Generate a truth (logic) table (using 0’s and 1’s) for equation (2) and then make a voltage table (using L’s and H’s) for this logic diagram. Generate a complete simulation (timing diagram) for this circuit (using Quartus) and verify that it matches the voltage table.

   Note: Voltage tables are helpful in verifying simulation outputs (since Quartus simulations display voltages, not logic values). Unfortunately, in Quartus simulation a “0” represents a low voltage and a “1” represents a high voltage.

   Compare the voltage table to the Quartus simulation to verify that the circuit does indeed implement the equation given.

4. Print and submit both the design and the simulation (with annotation) and also submit the two tables.

5. Again draw (by hand and then with Quartus) a circuit design for equation (3). Note that this equation has the same right-hand side as the equations (1) and (2). In this design you are not limited in your gate selection (except that the gates should be available in the chips of your lab kit).

   \[
   X = [ (A \cdot B) + (C + /D) ]
   \]

   Choose activation-levels for the inputs and outputs that will allow you to minimize the number of gates necessary. Do NOT simplify the equation: Draw the gates in such a way that the logic of the equation is apparent in the circuit, e.g., if you need a 2-input AND gate with bubbles at the inputs (a BAND2 in Quartus), draw the gate this way instead of as a NOR gate. Show intermediate inputs as in part 1. Unless otherwise stated, all hand-drawn and Quartus-generated circuits this semester must be drawn as described above.

   Note that Quartus includes only some of the mixed-logic circuit elements in its libraries. For instance, Quartus does not have a level-shifter with the bubble on the input side.
Generate a voltage table for this design. (Hint: The truth table should be the same as the one made in the previous section. Truth tables depend only on the logic equations, not on the logic design. Note that the simulation for this design will NOT match the simulation for the design of parts 1-4.) Submit the design, simulation, and voltage table. For this entire semester, when using Quartus to draw a circuit, label all active-low inputs or outputs with \_L at the end, since \_L and (L) will not work, e.g., R(L) will be written as R\_L. All active-high signals will end in \_H or have no special ending (your choice), e.g., S(H) will either be written as S\_H or S.

6. Copy the logic diagrams in Quartus for equations (2) and (3) and place them in a single new file, i.e., this file will have circuits for both W and X. Generate a complete timing diagram for these two circuits (with Quartus) and verify that the voltage tables for the two circuits match the simulation outputs. Since all of the inputs for the positive-logic circuit are active-high and some of the inputs for the mixed-logic solution are probably active-low, if you just copy the two files you will have eight inputs. In order to directly compare the outputs, use the four inputs for either W or X and create the other necessary inputs (with opposite activation-levels) using level-shifters as shown in Figure 1. Print out both the design and the simulation.

\[
\begin{align*}
G(H) & \quad G(L) \\
J(L) & \quad J(H)
\end{align*}
\]

Figure 1: Use only four inputs. Create alternate activation-level inputs with level-shifters.

7. Design mixed-logic implementations of the equations for Y and Z in equations (4) and (5) below. The goal in this part is to choose input and output activation-levels to minimize the total number gates and chips used in the overall design of these two circuits. Choose only one of the two possible activation-levels for each of the inputs, i.e., A(H), B(L), etc. [but not A(H) for one and A(L) for the other]. (If you need both A(H) and A(L), that will cost one gate, a level-shifter or its equivalent, as shown in Figure 1.) Do the design by hand and then do it with Quartus in a single file. Do not simplify. (Hint: No more than two chips are needed.) Add pin number and chip labels to each gate to change this schematic into a wiring diagram.

\[
Y = [ (A * B) + (C + D) ] \quad (4)
\]
\[
Z = [ (A + B) * (C * D) ] \quad (5)
\]

Print out both the design and the simulation.

8. Create a truth table for equations (4) and (5). Note: Activation-levels have no effect when constructing a truth table from a logic equation.

9. Create a voltage table for equations (4) and (5).

10. Add pin numbers and chip labels to your design in part 7. You may either add this text by hand or with Quartus.

11. For this lab only, you will also draw a layout of your circuit as it would appear on your protoboard. A layout shows each of the parts (ICs, switches, LEDs, SIP and DIP resistor packs) as they appear on the prototype board. Include the needed switches, resistors (SIP and/or DIP), and LED’s. Generally, we will not draw a layout in this course, but instead just place pin numbers and labels on a schematic diagram. (You should use one of the posted files: protoboard_for_layout.ppt [a PowerPoint file] or protoboard_for_layout.pdf [an Acrobat file] to draw your layout.)

Draw a layout of the circuit you designed in parts 7 and 10 of the Pre-Lab (above).

In future labs you will draw logic circuit diagrams (also known as schematic circuit diagrams) with pin numbers added as you did in part 10 above, but will NOT draw layout diagrams.

Note: You are asked to construct these circuits below in the next section.

Note: For the remainder of the semester, all circuits should be simulated and the simulation output should be compared to the voltage table to verify that the circuit performs the required function(s). In every lab, part of the pre-lab requirements is to turn in your truth tables, voltage tables, Quartus design printouts and Quartus simulations printouts. Also, for this lab and all other labs this semester, submit your design and simulation work [in Quartus archive file(s)] by email (as described in the syllabus) BEFORE entering the lab.

**PROCEDURE**

1. Show the TA your pre-lab work (i.e., hand drawn designs, tables, and printouts of the Quartus circuit and timing diagrams).

2. Implement the pre-lab’s wiring diagrams for both circuits in pre-lab part 7 on your own protoboard. You are encouraged to wire your protoboard with your own wires and to do as much as possible at home (before lab). All inputs must come from switches and all outputs must go to LED’s (as described in lab 1 and the Hardware: Getting Started document). The activation-level of each input must be obvious for each of the inputs. There are two ways to accomplish this. The first (see Figure 2) is to
make a legend either on your circuit board or as a legend on your design that indicates the switch position for each input signal when it is true. The other technique requires the use of two switch banks, one for active-high inputs and one for active-low inputs. In this technique, up should be true for both switches. For this semester, I would like you to use the first technique, i.e., draw a legend on your design. On **ALL** your wiring diagrams this semester, draw a picture of a switch including the word ON. All output LED circuits should match the activation-level of the corresponding output. An LED should be on (lit) when the corresponding output is true.

3. Demonstrate the operation of the circuits you built by switching through various inputs and comparing the output LED results to those obtained in the pre-lab simulation.

**Special Notes**

- If you need help with this lab, don’t hesitate to ask questions in class, visit a professor, or visit a TA during office hours.
- There will be a 45-minute to 1 hour quiz relating to lab 1 and the pre-lab at the beginning of this lab. Quizzes may happen at the beginning of any lab. In general, lab quizzes will relate to previous labs or the lab you will do immediately following.

1) In this lab you will be given a new equation (similar to the two given in the pre-lab section).
   a) Draw the logic diagram by hand, using appropriate mixed-logic notation.
   b) Draw the circuit (in Quartus).
   c) Draw a truth table for the equation.
   d) Draw a voltage table for the equation.
   e) Verify the correct operation of the circuit using Quartus simulation and comparing this to your voltage table.
   f) Build the circuit and demonstrate its correct operation.
- You are encouraged to build and test your circuits at home. We have found that students who build their circuits at home get better grades than those who do not build their circuit before lab. At home there is not the same time pressure that can cause you to make silly mistakes that cause your circuit to operate improperly.

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**Figure 2:** Switch layout with true switch positions labeled. A and C are active-low signals; B and D are active-high signals. The A and D switches are in their true positions; the B and C switches are in their false positions.