What is DMA?

• Stands for Direct Memory Access.
• Hardware that is capable of high speed data transfers with minimal CPU intervention from:
  • Data memory to data memory
  • Data memory to peripheral
  • Peripheral to data memory
  • Peripheral to peripheral
• Can be triggered off numerous peripheral flags using the event system.
• Used to parallelize embedded code.
DMA Transactions

• DMA separates data into three types of transfers.
  • Burst
    • 1, 2, 4, or 8 byte long pieces of data that represent a single data element
    • This is an instantaneous transfer
  • Block
    • Group of data consisting of burst transfers. Adjustable from 1 byte to 64KB.
  • Transaction
    • Complete DMA transfer of n desired blocks

DMA Configuration

Table 5-4. Summary of triggers, transaction complete flag and channel disable according to DMA channel configuration.

<table>
<thead>
<tr>
<th>REPEAT</th>
<th>SINGLE</th>
<th>REPCNT</th>
<th>Trigger</th>
<th>Flag set after</th>
<th>Channel disabled after</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Block</td>
<td>1 block</td>
<td>1 block</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Block</td>
<td>1 block</td>
<td>1 block</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>n &gt; 1</td>
<td>Block</td>
<td>1 block</td>
<td>1 block</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>BURSTLEN</td>
<td>1 block</td>
<td>1 block</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>BURSTLEN</td>
<td>1 block</td>
<td>1 block</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>n &gt; 1</td>
<td>BURSTLEN</td>
<td>1 block</td>
<td>1 block</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Block</td>
<td>Each block</td>
<td>Each block</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Transaction</td>
<td>1 block</td>
<td>1 block</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>n &gt; 1</td>
<td>Transaction</td>
<td>n blocks</td>
<td>n blocks</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>BURSTLEN</td>
<td>Each block</td>
<td>Never</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>BURSTLEN</td>
<td>1 block</td>
<td>1 block</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>n &gt; 1</td>
<td>BURSTLEN</td>
<td>n blocks</td>
<td>n blocks</td>
</tr>
</tbody>
</table>
DMA Trigger Sources

- DMA can be triggered from software (by default), peripheral, or the event system.
- Setting CTRLA’s (5.14.1 AU Manual) TRFREQ bit trigger’s a software request for a DMA transfer.
- TRIGSRC (5.14.4 AU Manual) is used to select the peripheral or event system trigger source.
  - A base offset is given in table 5-9 for the specific peripheral.
  - If there are different flags for a given peripheral, additional offsets are given in tables 5-10, 5-11, 5-12 and/or 5-13.

DMA Addressing

- Two important addresses:
  - Source: Where the data is coming from
  - Destination: Where the data is going to
- Address may be incremented, decremented, or remain static after each burst transfer.
- Original Source and Destination addresses are stored inside DMA controller, and may be restored after:
  - Each Burst transfer
  - Each Block transfer
  - Each Transaction
  - Or never
DMA Protection

- Integrity of the transfers are maintained by the DMA Controller.
- If the CHnBUSY flag (bit) in STATUS (5.13.3 AU Manual) is set, the following are locked for that channel:
  - DMA CTRL register
  - DMA INTFLAGS register
  - CHEN, CHRST, TRFREQ, and REPEAT in CHn CTRL register
  - CHn TRIGSRC register
- To access these registers, simply disable the DMA channel register

DMA Interrupts

- Two types of interrupts per channel
  - Error (CHnERRIF[3:0] (5.13.2 AU Manual)) if an error condition is detected on the channel.
  - Transaction finished (CHnTRNIF[3:0] (5.13.2 AU Manual)) that will be set at the end of a transaction.
    - In the even of DMA being in repeat mode, CHnTRNIF will be set after each Block transfer.
Double Buffering

- Allows for continuous transfer by interlinking two channels so the second takes over when the first is finished, and vice versa.
  - May be set up using channels 0 and 1 as the first pair, or 2 and 3 as the second.

Data is being read into this buffer

```
488598932938200320
```

while data in this buffer is being processed.

```
7543994880000488048840MR88900032342
```

DMA Set-Up

- DMA Controller
  - CTRL (5.13.1 AU Manual)
    - Enable, buffer mode, priority

- DMA Channel
  - TRIGSRC (5.14.4 AU Manual)
    - Selecting trigger source (if any)
  - ADDRCTRL (5.14.3 AU Manual)
    - If/when to reload source/destination address
    - If to increment, decrement, or remain static after burst transfer
  - TRFCNT (5.14.5/6 AU Manual)
    - Number of byte transfers in a Block transfer
  - REPCNT (5.14.7 AU Manual)
    - How many times to repeat Block transfer (or how many blocks per transaction).
    - For unlimited repeats, set to 0.
DMA Set-Up

- DMA Channel
    - Where to start reading data from
    - Where to start writing data to

- DMA Channel Interrupts
  - CTRLB (5.14.2 AU Manual)
    - Error Interrupt Level/Transaction Interrupt Level