M68HC11 BASIC INSTRUCTION SET AND PROGRAMMERS MODEL

- *Data Movement:*

LDAA, LDAB, LDD	**STAA**, STAB, STD	PULA. PULB, PSHA, PSHB
LDS, LDX, LDY	STS, STX, STY	PULX, PULY, PSHX, PSHY
TAB, TBA, TAP, TPA	TSX, TXS, TSY, TYS, XGDX, XGDY	

- *Arithmetic/Logic/Shift:*

ABA, ADDA, ADDB, ADDD, ABX, ABY	ANDA, ANDB	LSLA, LSLB, LSL, LSLD=ASLD
SBA, SUBA, SUBB, SUBD,	ORAA, ORAB	LSRA, LSRB, LSR, LSRD
ADCA, ADCB	EORA, EORB	ASLA, ASLB, ASL, ASLD=LSLD
SBCA, SBCB		ASRA, ASRB, ASR
MUL, IDIV, FDIV		RORA, RORB, ROR
INCA, INCB, INC		ROLA, ROLB, ROL
DECA, DECB, DEC		
INX, INY, INS		
DEX, DEY, DES		
NEG, COM, DAA		

- *Decision Making:*

No Flag	Carry Flag	Zero Flag	Sign Flag	Overflow	Arithmetic	Logical
BRA	BCC, BCS	BEQ, BNE	BMI, BPL	BVS, BVC	BGE, BGT	BHI, BHS
JMP					BLE, BLT	BLO, BLS

- *More Decision Making:*

BIT, CBA, CMPA, CMPB, CPD, CPX, CPY, TST, BRSET, BRCLR, BSR, JSR, RTS, RTI

- *Miscellaneous :*

BCLR, BSET, CLRA, CLRB, CLR, CLC, SEC, CLV, SEV, CLI, SEI, NOP, STOP, SWI, WAI

- *Addressing Modes:*

Immediate:	The data value is included in the instruction {immediately follows the instruction opcode}.
Direct	The operand is the page 0 address of the data value.
Extended	The operand is the 16-bit address of the data value.
Indexed	The address of the data value is contained in Index Register X or Y.
Inherent	The opcode specifies the address of the data inside the CPU.
Relative	The destination of the branch instruction is specified relative to the address in the PC register.