UP-2 header installation and pin safety issues

It is recommended that each student solder four 2x30 male header to the four areas on the UP-2 board labeled *MAX_EXPAN* (for CPLD) and *FLEX_EXPAN_A* through *FLEX_EXPAN_C* (for FPGA). These headers will make LSA connection easier, since the FPGA does not have pins that easily attach to LSA leads. The CPLD's pins can be accessed through the inner ring of black female headers, but this requires small wires or a double-ended male header in order to connect to the LSA leads. The 2x30 male headers are not required for 4712 lab, but are highly recommended, as they save valuable in-lab time!

Procedure:

1) Be sure you have the UP-2 board face up, i.e. you have all the chips facing you when trying to locate the areas where the headers will be placed. The first is labeled *MAX_EXPAN* and is on the left side of the UP-2 board next to the CPLD (MAX) chip. The next three are labeled *FLEX_EXPAN_A* through *C* surround the right part of the board near the FPGA (FLEX) chip. The areas look like long rows of holes with solder pads surrounding each hole. Get or make a two row by 30-pin strip of male pins. These type pins are called "berg" headers. You can measure the header against the board holes to avoid counting.
2) Place two of the 1x30 headers or one of the 2x30 headers into the MAX_EXPANSION area, side by side, being sure to have the longer pins facing up, away from the board.
3) Hold the headers in place while turning the board upside down. Put a small amount of solder on the ends of each header (4 pins total) to hold the headers in place. Now solder the remaining pins, and make sure there are no visible shorts!! If you are unsure whether a short is present, use a meter to test. Shorts could permanently damage either chip.
4) Do the same for the other headers, placed on the FLEX_EXPAN_C area.

Pin Safety Issues

Since most pins on the CPLD and FPGA chips can be programmed as either inputs or outputs, students must be careful to avoid connecting outputs together. As a general rule, whenever programming the CPLD or FPGA with a different program, **DETACH ALL WIRES CONNECTING THE CHIP TO ANY EXTERNAL SOURCES**. This also applies to any wires from the headers to the dip switches. If you only modified the code slightly and are SURE the pin assignments did not change, you may avoid detaching the wires. Once the new program is loaded, connect the wires up according to the new pin assignments. LSA connections can remain on the headers, as they are all inputs to the LSA.

Hard-wired connections

Students should be aware of the several hard-wired connections on the UP-2 board. These include the 7-segment LEDs, VGA port (FPGA only), and the PS/2 (mouse/keyboard) port (FPGA only). The single LEDs and dip switches are NOT hard-wired, but require a wire from the small, black female headers adjacent to the switch or LED. The UP-2 board has an on-board 25.175 MHz oscillator that is hard-wired to the FPGA and CPLD. Refer to the UP-2 manual for the exact pin assignments of the CPLD and FPGA. Generally speaking, an output should not be sent to a 7-segment pin unless the 7-segment display is specifically called for in the lab assignment. Experience has showed the 7-segment display pins can occasionally have ***odd*** effects when probed by the LSA, possibly because of the large current they draw.