Lab 0-1: Word Generator and Introduction to the LSA and Oscilloscope

PURPOSE
The purpose of this lab is to introduce the software and hardware development tools used in EEL 4712 to design, construct and test digital circuits. In labs 0 and 1 you will design, simulate, build and demonstrate two 8-bit word generators (counters), one with discrete IC’s (lab 0) and the other with an FPGA (lab 1). The specific skills pertaining to this lab are test vector generation, system design testing and verification, and the understanding of how to use a logic analyzer (LSA) and an oscilloscope. This lab also reintroduces the Altera Quartus software package and introduces the Bin-Tek BT-U circuit board.

MATERIALS
- Protoboard (hopefully yours from EEL 3701)
- Wire kit (yours from EEL 3701)
- Two 74HC163 IC’s (given to you in lab)
- Clock generator (may be available for in lab use)
- 2 bypass capacitors (0.1 µF)
- For lab 1:
  - Bin-Tek BT-U Board
  - ByteBlaster Cable (yours from your BT-U kit or from another source)
  - Soldering iron (provided)
  - Jumpers (provided)
- Following document printouts:
  - This lab handout
  - Lab rules and policies
  - Relevant parts of 74’163 spec sheets
- For lab 1:
  - BT-U User’s Manual
  - BT-U Quartus Test Manual
  - BT-U FAQ
- Software copies needed (printouts optional)
  - LSA Tutorial
  - Oscilloscope Tutorial
  - Oscilloscope User’s Manual
- Oscilloscope (in lab)
- Logic Analyzer (in lab)
- Flash (thumb drive) or 3.5” Floppy disk is needed to grab LSA info.
- Flash, floppy or CD of your work [Note: No CD writer in lab]

STUDENT INFO
For this lab and subsequent labs, put your name and section number as a comment at the beginning of all VHDL files and in a title block in all graphic design files (.bdf). See the “Lab rules and policies” handout for more information.

PRELAB REQUIREMENTS
Design an 8-bit "word generator" using the two 74HC163 chips. The data sheet for this part can be found on the class website. The word generator should be implemented as a synchronous (common clock) 8-bit counter. Save yourself lab time by doing the wiring for the 8-bit word generator at home, leaving space for the two 74HC163’s that will be distributed at the start of this lab.

1. Read/scan the Acute LSA LA2132P User's Manual (available from the class website).
2. Read Tutorial 1 (Appendix B) and Tutorial 2 (Appendix C) in your textbook. (The old textbook discusses MaxPlusII; the new one discusses Quartus.) This provides a good overview of Quartus and how to program devices. It would be very beneficial to actually perform the tutorial examples yourself in Quartus. My tutorial (on our website) would be a good place to start.
3. Refer to the data sheet for the 74HC163 for information on part operation and specifications. Figure 11 in the Motorola spec sheet shows how to create an n-bit synchronous counter. Use the Quartus graphic editor to draw a mixed-logic circuit diagram of an 8-bit word generator constructed using two 74HC163 devices. (Double-click on a blank area of the graphic editor and select 74163 from the altera/quartus41/libraries/others/maxplus2 directory.) Add pin numbers to make this a wiring diagram. Don’t put the pin numbers too close to the wires (or Quartus will get confused and think these are wire names). Note: Put your name (using Quartus) on all files throughout the semester. (See “Lab rules and policies” for more info.)
4. Determine the settings needed for the various input pins (reset, enable P, …) that will allow the counter to run continuously. Prepare test inputs using the Quartus Waveform Editor. Display all inputs and outputs as well as the signal from the internal ripple carry output that allows the second counter to count. Simulate the counter to verify that it indeed serves as an 8-bit word generator that can provide a sequence of 8-bit binary numbers in the order appropriate to a canonical truth table.
5. Read the BT-U Board manual to become familiar with the hardware. If you have not yet received your board, this manual is located on the Bin-Tek website and on the class website under Software/Docs.
6. Assign the device "Cyclone | EP1C3T144C8". Compile the circuit. Fix any errors until the design compiles properly.
7. In the Quartus waveform simulation, zoom in on the region where the first counter causes the second counter to count, e.g., 0000 1111 to 0001 0000. Obtain a printout of this region.

8. Print the schematic to help you construct the circuit and bring it to lab.

9. When doing lab 1 and programming your BT-U board, use the Floorplan Editor to make FPGA pin assignments for all inputs and outputs and recompile the project.

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**IN-LAB PROCEDURE FOR LAB 0**

1. Get your parts from the TA.

2. Give your TA the filled out form called *Lab rules and policies*. You will use the password to view your grades throughout the semester. Keep it private unless you want others to know your grades. **Write it down and save it.**

3. Be sure that your power supply is **NOT** plugged in during this step. Construct the 8-bit word generator using the parts provided by the Lab Instructor. Connect a power bypass capacitor (0.1µF) between Vcc and GND of each device. Keep the leads of the capacitor short. The parts provided on the conductive foam are yours to keep and use for this and other lab assignments. Be sure to keep the parts on the foam except when they are in use in order to protect them from static discharge damage.

4. After you have double-checked your wiring and you are **POSITIVE** the circuit is correct, apply power. Set the clock input at a relatively high frequency (~100kHz) as supplied by the protoboard in lab by using the oscillator provided in lab. (You must return this part to the TA at the end of your lab.) Be sure to connect the protoboard ground to your circuit ground. (Alternatively, you can use the 25MHz clock available on your BT-U board, if you have yours.)

5. With the counter-based word generator supplying an ascending binary code (hopefully), explore the word generator using the oscilloscope. Connect the ground connection of the oscilloscope probe directly to the ground pin of the 74HC163 under test. Synchronize channel A of the scope to the rising edge of the ripple carry output (RCO) of the digit under test. Observe the values on the other bits of the outputs of the selected digit with channel B.

6. Make a drawing (or take a digital picture with **YOUR** camera) of each output for the selected digit as seen on the oscilloscope. Preserve and record the time relationship between the signals and the clock. The drawing should show the clock trace across the top. The signals QA, QB, QC, QD, (Q0-Q3, respectively) and RCO should follow below. A vertical line parallel to a rising edge of the clock signal should correspond to the same time in each of the other traces. The drawing will be made with pencil and paper (or with **YOUR** digital camera) in the lab. Include this drawing in your lab write-up. Be sure to reproduce the small deviations of the observed signal from a perfect square wave. Make a similar drawing for the other digit.

7. Temporarily move the ground probe from the IC ground and leave it floating. Make a drawing (or take a digital picture) of one or two cycles of the QA trace on the least significant digit of the word generator. Now connect the ground probe to the ground pin on the protoboard power supply. Make a drawing (or take a digital picture) of one or two cycles of the QA trace on the least significant digit of the word generator. Check that the waveform changed from that obtained when it was connected to the IC ground. The deviation will be discussed in the questions.

8. Measure the time delay from the clock’s rising edge to the rising edge of each Q output in the 8-bit word generator. Make small sketches (annotate the drawing or picture) that show the points on the waveform that are being used for the measurement. Prepare a table of the measured parameters. You may need to adjust the oscilloscope to make the measurements more accurate. These are the clock frequency and the oscilloscope horizontal time base period. What delay do you expect from the clock edge to each Q output? Should this delay be dependent upon the Q output being observed? Record the sweep rate that yielded the most accurate measurement.

9. Remove the oscilloscope connections from the 8-bit word generator. Connect the LSA in such a way that it can acquire data on each rising edge of the word generator’s clock (synchronous data acquisition). Connect additional leads to all of the outputs of the word generator including the two RCO signals.
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Group the signals on the pods in such a way that the Q outputs can be grouped and viewed as hexadecimal numbers. Additional information about the LSA can be found on the class.

1. Connect the LSA to the 8-bit counter. The clock input to the counter should serve as the clock input to the LSA. Connect 8 data wires from the LSA pod to the 8 outputs of the counter. Also connect two LSA data wires to the RCO pins of the 74HC163s to show how the count propagates from one device to the next. Set the LSA to trigger when the count is all 0’s and display the state in binary. Save the state listing from %11101000 (SE8) to %00001000 (S08) to a floppy and include it in the final report.

2. Switch the LSA to the timing waveform display. Adjust the display until the values from $00 to $80 are displayed. Save the screen to a floppy. To save the image, use either “Print Screen” or save it as a bitmap (.BMP) file. Readjust the display so the display includes $70 to $FF. Save the screen to a floppy.

3. Acquire a complete cycle of the data (at least 256 samples) in sync with the rising edge of the clock. Arrange the LSA data formatting such that the data is shown in binary and in hexadecimal form in a text display. Save the data to the disk. Perform a similar run and acquire the data in a waveform display. Does the clock signal’s display show a square wave? Account for what you see.

4. Repeat the LSA acquisition using the falling edge of the clock as a trigger. Record a complete cycle of the data (at least 256 samples) in sync with the rising edge of the clock. Arrange the LSA data formatting such that the data is shown in binary and in hexadecimal form in a text display. Save the data to the disk. Perform a similar run and acquire the data in a waveform display. Does the clock signal’s display show a square wave? Account for what you see.

5. Repeat steps 5-12 of the In-Lab Procedure for Lab 0 and note any differences in the lab report.

QUESTIONS

1. The device used to construct the word generator has the designator 74HC163. What is the meaning of the "HC" in the designator? A character is normally placed immediately following the designator, which is called the "suffix" in the data sheet. The parts in the lab have plastic cases with pins arranged down the long sides. The pin spacing is 0.1 inch and the rows of pins are spaced 0.3 inches apart. What suffix do you expect to find on the designator for the devices used in the lab? What is the propagation time from the clock to the Q outputs and RCO for the part type used in the lab?

2. Figure 12 in the Motorola data sheet for the 74HC163 describes a "Nibble Ripple Counter". Describe the major difference between this counter and the one used as the word generator above. With the help of Figure 1 and tPLH for the “Minimum Propagation Delay, Clock to Ripple Carry Out,” contrast the behavior of the outputs of the two nibbles for an 8-bit counter built as in Figure 11 with that of an 8-bit counter built as in Figure 12. Assume the power supply voltage is +5V, the temperature is 25 °C, and the clock frequency is essentially 30 MHz with a 50% duty cycle. We are specifically interested in the events that happen and their timing when the left-most 4-bit counter transitions from 1111 to 0000 and the right-most 4-bit counter increments (major carry). What are the values on the outputs of these counters through the period specified and how long do the outputs stay valid? Are some output combinations held longer than others? Are there any combinations that occur "out of order"? Remember that our goal was to design a network that produced values that could be used to build a canonical truth table.

IN-LAB PROCEDURE FOR LAB 1

1. Solder your Byte Blaster header and four long headers onto your BT-U board. Some soldering irons will be provided in lab, but feel free to do this on your own at home. A soldering guide will be available on the Bin-Tek website.

2. You can skip this step for the sake of time; but, for your benefit, be sure to do it before lab 2. Test your BT-U board with the test procedure on the Bin-Tek website described in the document BT-U Quartus Test Manual with the software in the BT-U Quartus Test Program.
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3. The 8-bit word generator was designed using the 74HC163. It was implemented in the lab using a specific model of the IC. One of the parameters in the suffix described the package type. The next parameter describes the speed and temperature grade of the device. What is the complete part number that was used in the lab? What is the speed grade of the part? What is the temperature range over which the device characteristics are valid? Compare the value measured for the propagation time for the "major carry" described in question 2 with the value given for the part in the 74HC163 data sheet.

4. The part used to contain the design for simulation in the pre-lab work was a FPGA. Specify the package style, number of pins, speed and temperature grade of the part used. In the simulation work done during pre-lab, measure the "major carry" time. Compare the value obtained with that discussed in question 3.

5. Discuss any changes that occurred in the waveform as seen on the oscilloscope when the probe’s ground connection was moved from the device ground pin to the prototype board’s ground pin. Account for any changes.

6. Data was acquired by the LSA using both the rising-edge and the falling-edge of the clock. Were there any differences?

7. Describe the differences in the information acquired by the LSA and the oscilloscope. These differences include the number of channels and many others. Some of the features of an instrument allow you to determine if you meet the conditions for using the "digital domain". Others are useful only if the circuit is operating in the "digital domain". What is the "digital domain"?

LAB REPORT FORMAT
Final reports are due at the beginning of your next scheduled lab. These reports should include all of the sections listed on the Lab Guidelines in the Syllabus. The is also an example lab report available on the web site lab page.

The lab report is a formal document that describes the design, procedures, results and conclusions of the lab. The purpose is to convince the reader that the project is properly designed, tested, and meets its specifications. The lab report must be a well-organized computer-generated (printed, not hand written) document.

The title page should contain the following information:
   Lab Number: Lab Title
   Student Name
   EEL 4712 Section Number

   Lab Meeting Date and Time
   Name of TA

The INTRODUCTION section of the report introduces, identifies and describes the project being designed. It describes the purpose of the lab.

The second section (DESIGN) will contain the design and validation material for the lab. Most projects can be divided into logical subsections and explained individually. Logic diagrams, flowcharts and other design information are placed in this section.

The next section (SIMULATION) will contain simulation results. For some labs, this may be included in the DESIGN section. Each logical subsection of a design must be simulated, if possible. Also include schematics and waveforms from Quarts Maxplus2.

The next section (TEST & VERIFICATION) third section deals with the preparation and testing of the complete system. Testing strategies and supporting data should be included from the physical testing of the project. The test procedures are described and results are given. The goal of this section is to convince the reader that the specified system design works according to the specifications. Your discussion of the test methods used is crucial. Use the hardware test output data and timing diagrams to show that the tests agree with the design specification. Oscilloscope drawings may be done by hand.

A final concluding section (CONCLUSION) is then given to summarize the complete design description. Include the answers to the lab questions as a separate section. Be sure to number each question response.

An appendix will be necessary for most labs to contain complete test data, VHDL code or other large documents. You should refer to the appendix or related figures when necessary, in the body of the report.

Feel free to add any additional sections that may be necessary to fully explain the lab.

The final report must not be hand written. Carefully choose a word processing system that can insert graphic images (the timing waveforms) and plain text tables of data (the state listings). I use Microsoft Word, but WordPerfect™, LaTeX and FrameMaker are also popular.