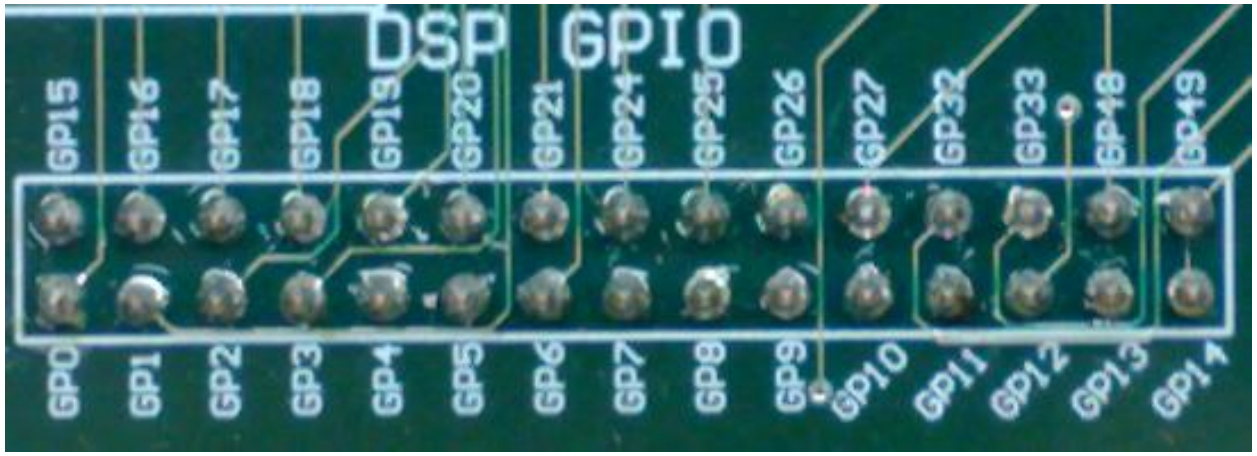
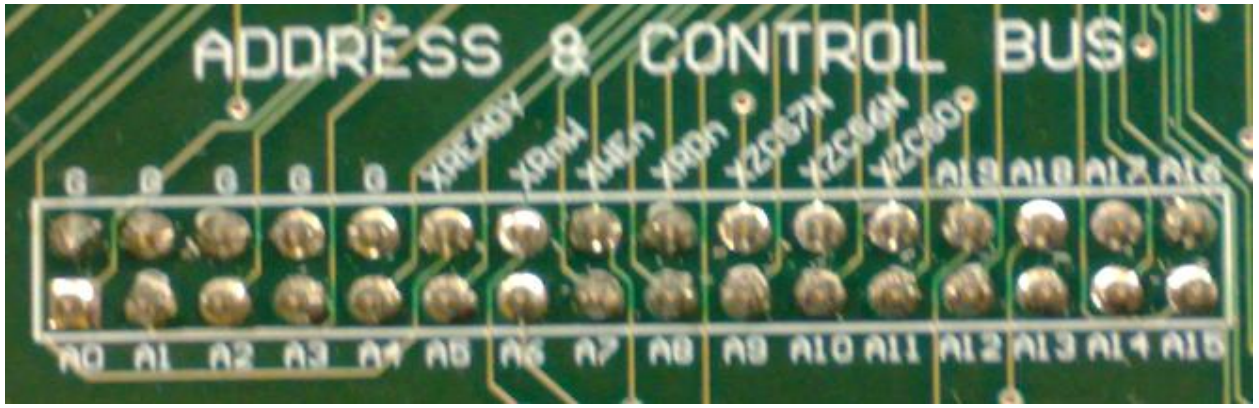
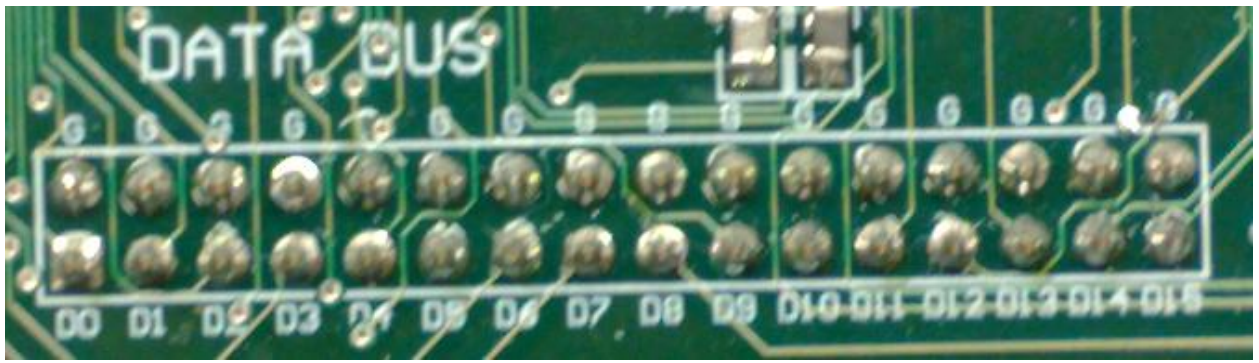
Header Definitions



Access to DSP GPIO Pins
(General Purpose I/O)

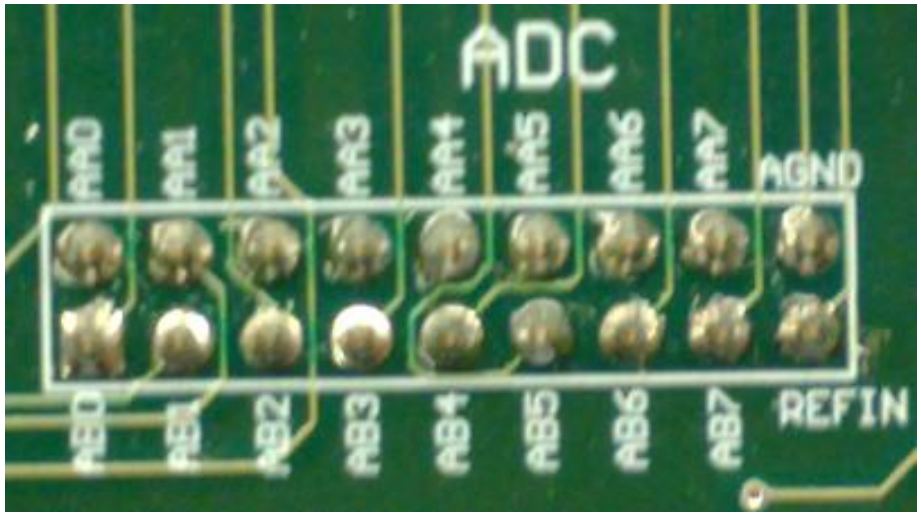


Access to DSP Address bus
and control bus



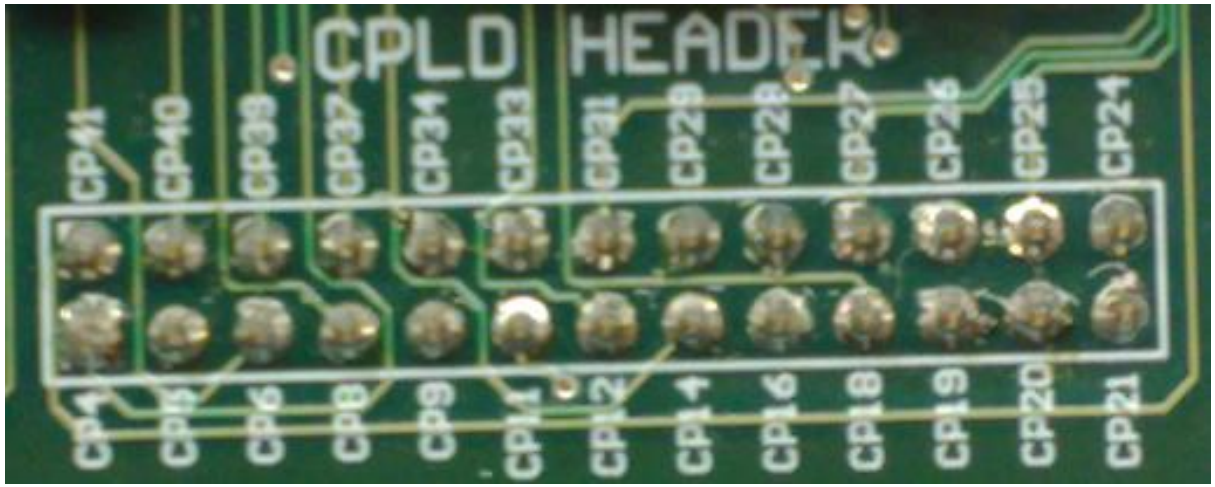
Access to DSP Data bus
and ground pins

Header Definitions (continued)



Access to DSP Analog to Digital Converter (ADC)

CPLD JTAG for programming an Altera EPM3064ALC44-10 CPLD if populated



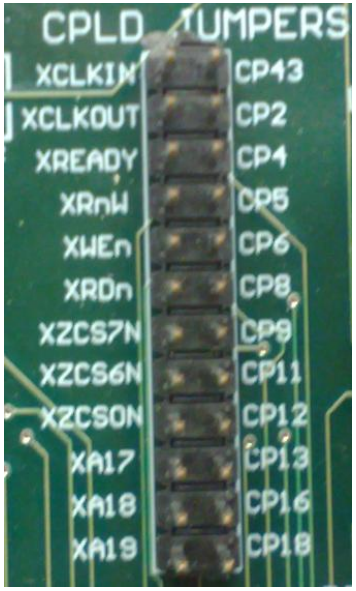
Access to CPLD pins (actual EPM3064ALC44 pin number)

Jumper Definitions

This position used when powering using **Ext Pwr (+5V)** Header

This position used when powering from XDS-100 USB

This position used when powering from DSP UART USB



Jumpers between DSP signals and hardwired CPLD pins