4 Register Block

The register block can be mapped to any 2-Kbyte boundary within the standard 64-Kbyte address space by manipulating bits REG[15:11] in the INITRG register. INITRG establishes the upper five bits of the register block's 16-bit address. The register block occupies the first 512 bytes of the 2-Kbyte block. Default addressing (after reset) is indicated in the table below. For additional information refer to **5 Operating Modes and Resource Mapping**.

Table 8 MC68HC912B32 Register Map (Sheet 1 of 5)

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
$0000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA[1]
$0001	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	PORTB[1]
$0002	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	DDRA[1]
$0003	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB[1]
$0004	0	0	0	0	0	0	0	0	Reserved
$0005	0	0	0	0	0	0	0	0	Reserved
$0006	0	0	0	0	0	0	0	0	Reserved
$0007	0	0	0	0	0	0	0	0	Reserved
$0008	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	PORTE[2]
$0009	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	0	0	DDRE[2]
$000A	NDBE	0	PIPOE	NECLK	LSTRE	RDWE	0	0	PEAR[2]
$000B	SMODN	MODB	MODA	ESTR	IVIS	EBSWAI	0	EME	MODE[3]
$000C	0	0	0	PUPE	0	0	PUPB	PUPA	PUCR[3]
$000D	0	0	0	0	RDPE	0	RDPB	RDPA	RDRIV[3]
$000E	0	0	0	0	0	0	0	0	Reserved
$000F	0	0	0	0	0	0	0	0	Reserved
$0010	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	0	INITRM
$0011	REG15	REG14	REG13	REG12	REG11	0	0	MMSWAI	INITRG
$0012	EE15	EE14	EE13	EE12	0	0	0	EEON	INITEE
$0013	0	NDRF	RFSTR1	RFSTR0	EXSTR1	EXSTR0	MAPROM	ROMON	MISC
$0014	RTIE	RSWAI	RSBCK	0	RTBYP	RTR2	RTR1	RTR0	RTICTL
$0015	RTIF	0	0	0	0	0	0	0	RTIFLG
$0016	CME	FCME	FCM	FCOP	DISR	CR2	CR1	CR0	COPCTL
$0017	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
$0018	ITE6	ITE8	ITEA	ITEC	ITEE	ITF0	ITF2	ITF4	ITST0
$0019	ITD6	ITD8	ITDA	ITDC	ITDE	ITE0	ITE2	ITE4	ITST1
$001A	ITC6	ITC8	ITCA	ITCC	ITCE	ITD0	ITD2	ITD4	ITST2
$001B	0	0	0	0	0	ITC0	ITC2	ITC4	ITST3
$001C–$001D	0	0	0	0	0	0	0	0	Reserved
$001E	IRQE	IRQEN	DLY	0	0	0	0	0	INTCR
$001F	1	1	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0	HPRIO
$0020	BKEN1	BKEN0	BKPM	0	BK1ALE	BK0ALE	0	0	BRKCT0
$0021	0	BKDBE	BKMBH	BKMBL	BK1RWE	BK1RW	BK0RWE	BK0RW	BRKCT1
$0022	Bit 15	14	13	12	11	10	9	Bit 8	BRKAH

Table 8 MC68HC912B32 Register Map (Sheet 2 of 5)

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
$0023	Bit 7	6	5	4	3	2	1	Bit 0	BRKAL
$0024	Bit 15	14	13	12	11	10	9	Bit 8	BRKDH
$0025	Bit 7	6	5	4	3	2	1	Bit 0	BRKDL
$0026–$003F	0	0	0	0	0	0	0	0	Reserved
$0040	CON23	CON01	PCKA2	PCKA1	PCKA0	PCKB2	PCKB1	PCKB0	PWCLK
$0041	PCLK3	PCLK2	PCLK1	PCLK0	PPOL3	PPOL2	PPOL1	PPOL0	PWPOL
$0042	0	0	0	0	PWEN3	PWEN2	PWEN1	PWEN0	PWEN
$0043	Bit 7	6	5	4	3	2	1	Bit 0	PWPRES
$0044	Bit 7	6	5	4	3	2	1	Bit 0	PWSCAL0
$0045	Bit 7	6	5	4	3	2	1	Bit 0	PWSCNT0
$0046	Bit 7	6	5	4	3	2	1	Bit 0	PWSCAL1
$0047	Bit 7	6	5	4	3	2	1	Bit 0	PWSCNT1
$0048	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT0
$0049	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT1
$004A	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT2
$004B	Bit 7	6	5	4	3	2	1	Bit 0	PWCNT3
$004C	Bit 7	6	5	4	3	2	1	Bit 0	PWPER0
$004D	Bit 7	6	5	4	3	2	1	Bit 0	PWPER1
$004E	Bit 7	6	5	4	3	2	1	Bit 0	PWPER2
$004F	Bit 7	6	5	4	3	2	1	Bit 0	PWPER3
$0050	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY0
$0051	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY1
$0052	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY2
$0053	Bit 7	6	5	4	3	2	1	Bit 0	PWDTY3
$0054	0	0	0	PSWAI	CENTR	RDPP	PUPP	PSBCK	PWCTL
$0055	DISCR	DISCP	DISCAL	0	0	0	0	0	PWTST
$0056	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0	PORTP
$0057	DDP7	DDP6	DDP5	DDP4	DDP3	DDP2	DDP1	DDP0	DDRP
$0058–$005F	0	0	0	0	0	0	0	0	Reserved
$0060	0	0	0	0	0	0	0	0	ATDCTL0
$0061	0	0	0	0	0	0	0	0	ATDCTL1
$0062	ADPU	AFFC	ASWAI	0	0	0	ASCIE	ASCIF	ATDCTL2
$0063	0	0	0	0	0	0	FRZ1	FRZ0	ATDCTL3
$0064	0	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0	ATDCTL4
$0065	0	S8CM	SCAN	MULT	CD	CC	CB	CA	ATDCTL5
$0066	SCF	0	0	0	0	CC2	CC1	CC0	ATDSTAT
$0067	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0	ATDSTAT
$0068	SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2	ATDTSTH
$0069	SAR1	SAR0	RST	TSTOUT	TST3	TST2	TST1	TST0	ATDTSTL
$006A–$006E	0	0	0	0	0	0	0	0	Reserved

Table 8 MC68HC912B32 Register Map (Sheet 3 of 5)

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
$006F	PAD7	PAD6	PAD5	PAD4	PAD3	PAD2	PAD1	PAD0	PORTAD
$0070	Bit 7	6	5	4	3	2	1	Bit 0	ADR0H
$0071	0	0	0	0	0	0	0	0	Reserved
$0072	Bit 7	6	5	4	3	2	1	Bit 0	ADR1H
$0073	0	0	0	0	0	0	0	0	Reserved
$0074	Bit 7	6	5	4	3	2	1	Bit 0	ADR2H
$0075	0	0	0	0	0	0	0	0	Reserved
$0076	Bit 7	6	5	4	3	2	1	Bit 0	ADR3H
$0077	0	0	0	0	0	0	0	0	Reserved
$0078	Bit 7	6	5	4	3	2	1	Bit 0	ADR4H
$0079	0	0	0	0	0	0	0	0	Reserved
$007A	Bit 7	6	5	4	3	2	1	Bit 0	ADR5H
$007B	0	0	0	0	0	0	0	0	Reserved
$007C	Bit 7	6	5	4	3	2	1	Bit 0	ADR6H
$007D	0	0	0	0	0	0	0	0	Reserved
$007E	Bit 7	6	5	4	3	2	1	Bit 0	ADR7H
$007F	0	0	0	0	0	0	0	0	Reserved
$0080	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0	TIOS
$0081	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0	CFORC
$0082	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0	OC7M
$0083	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0	OC7D
$0084	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (H)
$0085	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (L)
$0086	TEN	TSWAI	TSBCK	TFFCA	0	0	0	0	TSCR
$0087	0	0	0	0	0	0	0	0	TQCR
$0088	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4	TCTL1
$0089	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0	TCTL2
$008A	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A	TCTL3
$008B	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A	TCTL4
$008C	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I	TMSK1
$008D	TOI	0	PUPT	RDPT	TCRE	PR2	PR1	PR0	TMSK2
$008E	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F	TFLG1
$008F	TOF	0	0	0	0	0	0	0	TFLG2
$0090	Bit 15	14	13	12	11	10	9	Bit 8	TC0 (H)
$0091	Bit 7	6	5	4	3	2	1	Bit 0	TC0 (L)
$0092	Bit 15	14	13	12	11	10	9	Bit 8	TC1 (H)
$0093	Bit 7	6	5	4	3	2	1	Bit 0	TC1 (L)
$0094	Bit 15	14	13	12	11	10	9	Bit 8	TC2 (H)
$0095	Bit 7	6	5	4	3	2	1	Bit 0	TC2 (L)
$0096	Bit 15	14	13	12	11	10	9	Bit 8	TC3 (H)
$0097	Bit 7	6	5	4	3	2	1	Bit 0	TC3 (L)
$0098	Bit 15	14	13	12	11	10	9	Bit 8	TC4 (H)

Table 8 MC68HC912B32 Register Map (Sheet 4 of 5)

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
$0099	Bit 7	6	5	4	3	2	1	Bit 0	TC4 (L)
$009A	Bit 15	14	13	12	11	10	9	Bit 8	TC5 (H)
$009B	Bit 7	6	5	4	3	2	1	Bit 0	TC5 (L)
$009C	Bit 15	14	13	12	11	10	9	Bit 8	TC6 (H)
$009D	Bit 7	6	5	4	3	2	1	Bit 0	TC6 (L)
$009E	Bit 15	14	13	12	11	10	9	Bit 8	TC7 (H)
$009F	Bit 7	6	5	4	3	2	1	Bit 0	TC7 (L)
$00A0	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI	PACTL
$00A1	0	0	0	0	0	0	PAOVF	PAIF	PAFLG
$00A2	Bit 15	14	13	12	11	10	9	Bit 8	PACNT
$00A3	Bit 7	6	5	4	3	2	1	Bit 0	PACNT
$00A4–$00AC	0	0	0	0	0	0	0	0	Reserved
$00AD	0	0	0	0	0	0	TCBYP	PCBYP	TIMTST
$00AE	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0	PORTT
$00AF	DDT7	DDT6	DDT5	DDT4	DDT3	DDT2	DDT1	DDT0	DDRT
$00B0–$00BF	0	0	0	0	0	0	0	0	Reserved
$00C0	BTST	BSPL	BRLD	SBR12	SBR11	SBR10	SBR9	SBR8	SC0BDH
$00C1	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0	SC0BDL
$00C2	LOOPS	WOMS	RSRC	M	WAKE	ILT	PE	PT	SC0CR1
$00C3	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SC0CR2
$00C4	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF	SC0SR1
$00C5	0	0	0	0	0	0	0	RAF	SC0SR2
$00C6	R8	T8	0	0	0	0	0	0	SC0DRH
$00C7	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SC0DRL
$00C8–$00CF	0	0	0	0	0	0	0	0	Reserved
$00D0	SPIE	SPE	SWOM	MSTR	CPOL	CPHA	SSOE	LSBF	SP0CR1
$00D1	0	0	0	0	0	0	SSWAI	SPC0	SP0CR2
$00D2	0	0	0	0	0	SPR2	SPR1	SPR0	SP0BR
$00D3	SPIF	WCOL	0	MODF	0	0	0	0	SP0SR
$00D4	0	0	0	0	0	0	0	0	Reserved
$00D5	Bit 7	6	5	4	3	2	1	Bit 0	SP0DR
$00D6	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	PORTS
$00D7	DDS7	DDS6	DDS5	DDS4	DDS3	DDS2	DDS1	DDS0	DDRS
$00D8–$00DA	0	0	0	0	0	0	0	0	Reserved
$00DB	0	RDPS2	RDPS1	RDPS0	0	PUPS2	PUPS1	PUPS0	PURDS
$00DC–$00EF	0	0	0	0	0	0	0	0	Reserved
$00F0	1	1	1	1	1	EESWAI	PROTLCK	EERC	EEMCR
$00F1	1	1	1	BPROT4	BPROT3	BPROT2	BPROT1	BPROT0	EEPROT

Table 8 MC68HC912B32 Register Map (Sheet 5 of 5)

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
$00F2	EEODD	EEVEN	MARG	EECPD	EECPRD	0	EECPM	0	EETST
$00F3	BULKP	0	0	BYTE	ROW	ERASE	EELAT	EEPGM	EEPROG
$00F4	0	0	0	0	0	0	0	LOCK	FEELCK
$00F5	0	0	0	0	0	0	0	BOOTP	FEEMCR
$00F6	FSTE	GADR	HVT	FENLV	FDISVFP	VTCK	STRE	MWPR	FEETST
$00F7	0	0	0	FEESWAI	SVFP	ERAS	LAT	ENPE	FEECTL
$00F8	IMSG	CLKS	R1	R0	0	0	IE	WCM	BCR1
$00F9	0	0	I3	I2	I1	I0	0	0	BSVR
$00FA	ALOOP	DLOOP	RX4XE	NBFS	TEOD	TSIFR	TMIFR1	TMIFR0	BCR2
$00FB	D7	D6	D5	D4	D3	D2	D1	D0	BDR
$00FC	ATE	RXPOL	0	0	BO3	BO2	BO1	BO0	BARD
$00FD	0	0	0	0	0	BDLCEN	DLCPUE	DLCRDV	DLCSCR
$00FE	0	PDLC6	PDLC5	PDLC4	PDLC3	PDLC2	PDLC1	PDLC0	PORTDLC
$00FF	0	DDDLC6	DDDLC5	DDDLC4	DDDLC3	DDDLC2	DDDLC1	DDDLC0	DDRDLC
$0100–$01FF	0	0	0	0	0	0	0	0	Reserved

NOTES:

1. Port A, port B, and data direction registers DDRA and DDRB are not in map in expanded and peripheral modes.
2. Port E and DDRE not in map in peripheral mode; also not in map in expanded modes with EME set.
3. Not in map in peripheral mode.