2.2 Registers

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA) See page 88.	Read:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Write:								
		Reset:	U	U	U	U	U	U	U	U
$0001	Port B Data Register (PORTB) See page 89.	Read:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		Write:								
		Reset:	U	U	U	U	U	U	U	U
$0002	Data Direction Register A (DDRA) See page 89.	Read:	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0003	Data Direction Register B (DDRB) See page 90.	Read:	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0004	Reserved		R	R	R	R	R	R	R	R
↓										
$0007	Reserved		R	R	R	R	R	R	R	R
$0008	Port E Data Register (PORTE) See page 90.	Read:	PE7	PE6	PE5	PD4	PD3	PD2	PD1	PD0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0009	Data Direction Register E (DDRE) See page 91.	Read:	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	0	0
		Write:								
		Reset:	0	0	0	0	1	0	0	0
$000A	Port E Assignment Register (PEAR) See page 92.	Read:	NDBE	CGMTE	PIPOE	NECLK	LSTRE	RDWE	0	0
		Write:								
		Reset:	1	0	0	1	0	0	0	0
$000B	Mode Register (MODE) See page 81.	Read:	SMODN	MODB	MODA	ESTR	IVIS	EBSWAI	0	EME
		Write:								
		Reset:	0	0	0	1	1	0	0	1
$000C	Pullup Control Register (PUCR) See page 94.	Read:	0	0	0	PUPE	0	0	PUPB	PUPA
		Write:								
		Reset:	0	0	0	1	0	0	0	0
$000D	Reduced Drive Register (RDRIV) See page 95.	Read:	0	0	0	0	RDPE	0	RDPB	RDPA
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000E	Reserved		R	R	R	R	R	R	R	R

= Unimplemented R = Reserved U = Unaffected

Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 1 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$000F	Reserved		R	R	R	R	R	R	R	R
$0010	RAM Initialization Register (INITRM) See page 83.	Read:	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	0
		Write:								
		Reset:	0	0	0	0	1	0	0	0
$0011	Register Initialization Register (INITRG) See page 82.	Read:	REG15	REG14	REG13	REG12	REG11	0	0	MMSWAI
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0012	EEPROM Initialization Register (INITEE) See page 83.	Read:	EE15	EE14	EE13	EE12	0	0	0	EEON
		Write:								
		Reset:	0	0	0	1	0	0	0	1
$0013	Miscellaneous Mapping Control Register (MISC) See page 84.	Read:	0	NDRF	RFSTR1	RFSTR0	EXSTR1	EXSTR0	MAPROM	ROMON
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0014	Real-Time Interrupt Control Register (RTICTL) See page 124.	Read:	RTIE	RSWAI	RSBCK	0	RTBYP	RTR2	RTR1	RTR0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0015	Real-Time Interrupt Flag Register (RTIFLG) See page 125.	Read:	RTIF	0	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0016	COP Control Register (COPCTL) See page 125.	Read:	CME	FCME	FCM	FCOP	DISR	CR2	CR1	CR0
		Write:								
		Reset:	0	0	0	0	0	0	0	1
$0017	Arm/Reset COP Timer Register (COPRST) See page 127.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0018	Reserved		R	R	R	R	R	R	R	R
↓										
$001D	Reserved		R	R	R	R	R	R	R	R
$001E	Interrupt Control Register (INTCR) See page 72.	Read:	IRQE	IRQEN	DLY	0	0	0	0	0
		Write:								
		Reset:	0	1	1	0	0	0	0	0
$001F	Highest Priority I Interrupt Register (HPRIO) See page 73.	Read:	1	1	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
		Write:								
		Reset:	1	1	1	1	0	0	1	0

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Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 2 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0020	Breakpoint Control Register 0 (BRKCT0) See page 329.	Read: Write:	BKEN1	BKEN0	BKPM	0	BK1ALE	BK0ALE	0	0
		Reset:	0	0	0	0	0	0	0	0
$0021	Breakpoint Control Register 1 (BRKCT1) See page 330.	Read: Write:	0	BKDBE	BKMBH	BKMBL	BK1RWE	BK1RW	BK0RWE	BK0RW
		Reset:	0	0	0	0	0	0	0	0
$0022	Breakpoint Address Register High (BRKAH) See page 332.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
$0023	Breakpoint Address Register Low (BRKAL) See page 332.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$0024	Breakpoint Data Register High (BRKDH) See page 332.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
$0025	Breakpoint Data Register Low (BRKDL) See page 333.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$0026	Reserved		R	R	R	R	R	R	R	R
↓										
$003F	Reserved		R	R	R	R	R	R	R	R
$0040	PWM Clocks and Concatenate Register (PWCLK) See page 135.	Read: Write:	CON23	CON01	PCKA2	PCKA1	PCKA0	PCKB2	PCKB1	PCKB0
		Reset:	0	0	0	0	0	0	0	0
$0041	PWM Clock Select and Polarity Register (PWPOL) See page 136.	Read: Write:	PCLK3	PCLK2	PCLK1	PCLK0	PPOL3	PPOL2	PPOL1	PPOL0
		Reset:	0	0	0	0	0	0	0	0
$0042	PWM Enable Register (PWEN) See page 138.	Read:	0	0	0	0	PWEN3	PWEN2	PWEN1	PWEN0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0043	PWM Prescaler Counter Register (PWPRES) See page 139.	Read:	0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0044	PWM Scale Register 0 (PWSCAL0) See page 139.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 3 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0045	PWM Scale Counter Register 0 (PWSCNT0) See page 139.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0046	PWM Scale Register 1 (PWSCAL1) See page 140.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0047	PWM Scale Counter Register 1 (PWSCNT1) See page 140.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0048	PWM Channel Counter Register 0 (PWCNT0) See page 141.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0049	PWM Channel Counter Register 1 (PWCNT1) See page 141.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$004A	PWM Channel Counter Register 2 (PWCNT2) See page 141.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$004B	PWM Channel Counter Register 3 (PWCNT3) See page 141.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$004C	PWM Channel Period Register 0 (PWPER0) See page 142.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$004D	PWM Channel Period Register 1 (PWPER1) See page 142.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$004E	PWM Channel Period Register 2 (PWPER2) See page 142.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$004F	PWM Channel Period Register 3 (PWPER3) See page 142.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$0050	PWM Channel Duty Register 0 (PWDTY0) See page 143.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1

= Unimplemented R = Reserved U = Unaffected

Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 4 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0051	PWM Channel Duty Register 1 (PWDTY1) See page 143.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	1	1	1	1	1	1	1	1
$0052	PWM Channel Duty Register 2 (PWDTY2) See page 143.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	1	1	1	1	1	1	1	1
$0053	PWM Channel Duty Register 3 (PWDTY3) See page 143.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	1	1	1	1	1	1	1	1
$0054	PWM Control Register (PWCTL) See page 144.	Read:	0	0	0	PSWAI	CENTR	RDPP	PUPP	PSBCK
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0055	PWM Special Mode Register (PWTST) See page 145.	Read:	DISCR	DISCP	DISCAL	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0056	Port P Data Register (PORTP) See page 145.	Read: Write:	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0
		Reset:	U	U	U	U	U	U	U	U
$0057	Port P Data Direction Register (DDRP) See page 146.	Read: Write:	DDP7	DDP6	DDP5	DDP4	DDP3	DDP2	DDP1	DDP0
		Reset:	0	0	0	0	0	0	0	0
$0058	Reserved		R	R	R	R	R	R	R	R
↓										
$005F	Reserved		R	R	R	R	R	R	R	R
$0060	ATD Control Register 0 (ATDCTL0) See page 303.	Read: Write:	0	0	0	0	0	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$0061	ATD Control Register 1 (ATDCTL1) See page 303.	Read: Write:	0	0	0	0	0	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$0062	ATD Control Register 2 (ATDCTL2) See page 303.	Read:	ADPU	AFFC	AWAI	0	0	0	ASCIE	ASCIF
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0063	ATD Control Register 3 (ATDCTL3) See page 304.	Read:	0	0	0	0	0	0	FRZ1	FRZ0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

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Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 5 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0064	ATD Control Register 4 (ATDCTL4) See page 305.	Read: Write:	S10BM	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		Reset:	0	0	0	0	0	0	0	1
$0065	ATD Control Register 5 (ATDCTL5) See page 307.	Read: Write:		S8CM	SCAN	MULT	CD	CC	CB	CA
		Reset:	0	0	0	0	0	0	0	0
$0066	ATD Status Register (ATDSTAT) See page 309.	Read:	SCF	0	0	0	0	CC2	CC1	CC0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0067	ATD Status Register (ATDSTAT) See page 309.	Read:	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0068	ATD Test Register High (ATDTSTH) See page 310.	Read: Write:	SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2
		Reset:	0	0	0	0	0	0	0	0
$0069	ATD Test Register Low (ATDTSTL) See page 310.	Read: Write:	SAR1	SAR0	RST	TSTOUT	TST3	TST2	TST1	TST0
		Reset:	0	0	0	0	0	0	0	0
$006A ↓ $006E	Reserved		R	R	R	R	R	R	R	R
	Reserved		R	R	R	R	R	R	R	R
$006F	Port AD Data Input Register (PORTAD) See page 311.	Read: Write:	PAD7	PAD6	PAD5	PAD4	PAD3	PAD2	PAD1	PAD0
		Reset:	After reset, reflect the state of the input pins							
$0070	ATD Result Register 0 (ADRx0H) See page 311.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Undefined							
$0071	ATD Result Register 0 (ADRx0L) See page 312.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Undefined							
$0072	ATD Result Register 1 (ADRx1H) See page 312.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Undefined							
$0073	ATD Result Register 1 (ADRx1L) See page 312.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Undefined							

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Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 6 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0074	ATD Result Register 2 (ADRx2H) See page 312.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Undefined							
$0075	ATD Result Register 2 (ADRx2L) See page 312.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Undefined							
$0076	ATD Result Register 3 (ADRx3H) See page 312.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Undefined							
$0077	ATD Result Register 3 (ADRx3L) See page 312.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Undefined							
$0078	ATD Result Register 4 (ADRx4H) See page 312.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Undefined							
$0079	ATD Result Register 4 (ADRx4L) See page 312.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Undefined							
$007A	ATD Result Register 5 (ADRx5H) See page 312.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Undefined							
$007B	ATD Result Register 5 (ADRx5L) See page 312.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Undefined							
$007C	ATD Result Register 6 (ADRx6H) See page 312.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Undefined							
$007D	ATD Result Register 6 (ADRx6L) See page 312.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Undefined							
$007E	ATD Result Register 7 (ADRx7H) See page 312.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	Undefined							
$007F	ATD Result Register 7 (ADRx7L) See page 312.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Undefined							

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Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 7 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0080	Timer IC/OC Select Register (TIOS) See page 151.	Read: Write:	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
		Reset:	0	0	0	0	0	0	0	0
$0081	Timer Compare Force Register (CFORC) See page 151.	Read: Write:	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
		Reset:	0	0	0	0	0	0	0	0
$0082	Timer Output Compare 7 Mask Register (OC7M) See page 152.	Read: Write:	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
		Reset:	0	0	0	0	0	0	0	0
$0083	Timer Output Compare 7 Data Register (OC7D) See page 152.	Read: Write:	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
		Reset:	0	0	0	0	0	0	0	0
$0084	Timer Count Register High (TCNTH) See page 153.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0085	Timer Count Register Low (TCNTL) See page 153.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0086	Timer System Control Register (TSCR) See page 153.	Read: Write:	TEN	TSWAI	TSBCK	TFFCA				
		Reset:	0	0	0	0	0	0	0	0
$0087	Reserved		R	R	R	R	R	R	R	R
$0088	Timer Control Register 1 (TCTL1) See page 154.	Read: Write:	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
		Reset:	0	0	0	0	0	0	0	0
$0089	Timer Control Register 2 (TCTL2) See page 154.	Read: Write:	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
		Reset:	0	0	0	0	0	0	0	0
$008A	Timer Control Register 3 (TCTL3) See page 155.	Read: Write:	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
		Reset:	0	0	0	0	0	0	0	0
$008B	Timer Control Register 4 (TCTL4) See page 155.	Read: Write:	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 8 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$008C	Timer Mask Register 1 (TMSK1) See page 156.	Read: Write:	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
		Reset:	0	0	0	0	0	0	0	0
$008D	Timer Mask Register 2 (TMSK2) See page 156.	Read:	TOI	0	PUPT	RDPT	TCRE	PR2	PR1	PR0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$008E	Timer Interrupt Flag Register 1 (TFLG1) See page 157.	Read: Write:	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
		Reset:	0	0	0	0	0	0	0	0
$008F	Timer Interrupt Flag Register 2 (TFLG2) See page 158.	Read: Write:	TOF	0	0	0	0	0	0	0
		Reset:	0	0	0	0	0	0	0	0
$0090	Timer Input Capture/Output Compare 0 Register High (TC0H) See page 158.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
$0091	Timer Input Capture/Output Compare 0 Register Low (TC0L) See page 158.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$0092	Timer Input Capture/Output Compare 1 Register High (TC1H) See page 159.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
$0093	Timer Input Capture/Output Compare 1 Register Low (TC1L) See page 159.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$0094	Timer Input Capture/Output Compare 2 Register High (TC2H) See page 159.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
$0095	Timer Input Capture/Output Compare 2 Register Low (TC2L) See page 159.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$0096	Timer Input Capture/Output Compare 3 Register High (TC3H) See page 160.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
$0097	Timer Input Capture/Output Compare 3 Register Low (TC3L) See page 160.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 9 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0098	Timer Input Capture/Output Compare 4 Register High (TC4H) See page 160.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
$0099	Timer Input Capture/Output Compare 4 Register Low (TC4L) See page 160.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$009A	Timer Input Capture/Output Compare 5 Register High (TC5H) See page 160.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
$009B	Timer Input Capture/Output Compare 5 Register Low (TC5L) See page 160.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$009C	Timer Input Capture/Output Compare 6 Register High (TC6H) See page 160.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
$009D	Timer Input Capture/Output Compare 6 Register Low (TC6L) See page 160.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$009E	Timer Input Capture/Output Compare 7 Register High (TC7H) See page 161.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
$009F	Timer Input Capture/Output Compare 7 Register Low (TC7L) See page 161.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$00A0	Pulse Accumulator Control Register (PACTL) See page 161.	Read:	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00A1	Pulse Accumulator Flag Register (PAFLG) See page 163.	Read: Write:	0	0	0	0	0	0	PAOVF	PAIF
		Reset:	0	0	0	0	0	0	0	0
$00A2	Pulse Accumulator Count Register 3 (PACN3) See page 190.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$00A3	Pulse Accumulator Count Register 2 (PACN2) See page 190.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 10 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$00A4	Pulse Accumulator Count Register 1 (PACN1) See page 190.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$00A5	Pulse Accumulator Count Register 0 (PACN0) See page 190.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$00A6	16-Bit Modulus Down-Counter Control Register (MCCTL) See page 191.	Read: Write:	MCZI	MODMC	RDMCL	ICLAT	FLMC	MCEN	MCPR1	MCPR0
		Reset:	0	0	0	0	0	0	0	0
$00A7	16-Bit Modulus Down-Counter Flag Register (MCFLG) See page 192.	Read: Write:	MCZF	0	0	0	POLF3	POLF2	POLF1	POLF0
		Reset:	0	0	0	0	0	0	0	0
$00A8	Input Control Pulse Accumulators Control Register (ICPACR) See page 193.	Read: Write:	0	0	0	0	PA3EN	PA2EN	PA1EN	PA0EN
		Reset:	0	0	0	0	0	0	0	0
$00A9	Delay Counter Control Register (DLYCT) See page 193.	Read: Write:	0	0	0	0	0	0	DLY1	DLY0
		Reset:	0	0	0	0	0	0	0	0
$00AA	Input Control Overwrite Register (ICOVW) See page 194.	Read: Write:	NOVW7	NOVW6	NOVW5	NOVW4	NOVW3	NOVW2	NOVW1	NOVW0
		Reset:	0	0	0	0	0	0	0	0
$00AB	Input Control System Control Register (ICSYS) See page 194.	Read: Write:	SH37	SH26	SH15	HS04	TFMOD	PACMX	BUFEN	LATQ
		Reset:	0	0	0	0	0	0	0	0
$00AC	Reserved		R	R	R	R	R	R	R	R
$00AD	Timer Test Register (TIMTST) See page 196.	Read: Write:	0	0	0	0	0	0	TCBYP	PCBYP(1)
		Reset:	0	0	0	0	0	0	0	0
$00AE	Timer Port Data Register (PORTT) See page 196.	Read: Write:	PT7	PT6	PT5	PT4	PT3	PT2	PT1	PT0
		Reset:	0	0	0	0	0	0	0	0
$00AF	Data Direction Register for Timer Port (DDRT) See page 197.	Read: Write:	DDT7	DDT6	DDT5	DDT4	DDT3	DDT2	DDT1	DDT0
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 11 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$00B0	16-Bit Pulse Accumulator B Control Register (PBCTL) See page 197.	Read:	0	PBEN	0	0	0	0	PBOV	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00B1	Pulse Accumulator B Flag Register (PBFLG) See page 198.	Read:	0	0	0	0	0	0	PBOV	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00B2	8-Bit Pulse Accumulator Holding Register 3 (PA3H) See page 198.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00B3	8-Bit Pulse Accumulator Holding Register 2 (PA2H) See page 198.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00B4	8-Bit Pulse Accumulator Holding Register 1 (PA1H) See page 198.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00B5	8-Bit Pulse Accumulator Holding Register 0 (PA0H) See page 199.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00B6	Modulus Down-Counter Count Register (MCCNT) See page 199.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$00B7	Modulus Down-Counter Count Register (MCCNT) See page 199.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$00B8	Timer Input Capture Holding Register 0 (TC0H) See page 200.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	1	0	0	0	0	0
$00B9	Timer Input Capture Holding Register 0 (TC0H) See page 200.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00BA	Timer Input Capture Holding Register 1 (TC1H) See page 200.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00BB	Timer Input Capture Holding Register 1 (TC1H) See page 200.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 12 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$00BC	Timer Input Capture Holding Register 2 (TC2H) See page 201.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
$00BD	Timer Input Capture Holding Register 2 (TC2H) See page 201.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$00BE	Timer Input Capture Holding Register 3 (TC3H) See page 201.	Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Reset:	0	0	0	0	0	0	0	0
$00BF	Timer Input Capture Holding Register 3 (TC3H) See page 201.	Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	0	0	0	0	0	0	0
$00C0	SCI 0 Baud Rate Control Register High (SC0BDH) See page 206.	Read: Write:	BTST	BSPL	BRLD	SBR12	SBR11	SBR10	SBR9	SBR8
		Reset:	0	0	0	0	0	0	0	0
$00C1	SCI 0 Baud Rate Control Register Low (SC0BDL) See page 206.	Read: Write:	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		Reset:	0	0	0	0	0	1	0	0
$00C2	SCI Control Register 1 (SC0CR1) See page 207.	Read: Write:	LOOPS	WOMS	RSRC	M	WAKE	ILT	PE	PT
		Reset:	0	0	0	0	0	0	0	0
$00C3	SCI Control Register 2 (SC0CR2) See page 209.	Read: Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		Reset:	0	0	0	0	0	0	0	0
$00C4	SCI Status Register 1 (SC0SR1) See page 210.	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		Write:								
		Reset:	1	1	0	0	0	0	0	0
$00C5	SCI Status Register 2 (SC0SR2) See page 212.	Read:	0	0	0	0	0	0	0	RAF
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00C6	SCI Data Register High (SC0DRH) See page 213.	Read:	R8	T8	0	0	0	0	0	0
		Write:								
		Reset:	U	U	0	0	0	0	0	0
$00C7	SCI Data Register Low (SC0DRL) See page 213.	Read: Write:	R7T7	R6T6	R5T5	R4T4	R3T3	R2T2	R1T1	R0T0
		Reset:	Unaffected by reset							

= Unimplemented R = Reserved U = Unaffected

Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 13 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$00C8	Reserved		R	R	R	R	R	R	R	R
↓										
$00CF	Reserved		R	R	R	R	R	R	R	R
$00D0	SPI Control Register 1 (SP0CR1) See page 217.	Read:	SPIE	SPE	SWOM	MSTR	CPOL	CPHA	SSOE	LSBF
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00D1	SPI Control Register 2 (SP0CR2) See page 218.	Read:	0	0	0	0	PUPS	RDS	0	SPC0
		Write:								
		Reset:	0	0	0	0	1	0	0	0
$00D2	SPI Baud Rate Register (SP0BR) See page 219.	Read:	0	0	0	0	0	SPR2	SPR1	SPR0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00D3	SPI Status Register (SP0SR) See page 220.	Read:	SPIF	WCOL	0	MODF	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00D4	Reserved		R	R	R	R	R	R	R	R
$00D5	SPI Data Register (SP0DR) See page 221.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	Unaffected by reset							
$00D6	Port S Data Register (PORTS) See page 221.	Read:	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0
		Write:								
		Reset:	After reset all bits configured as general-purpose inputs							
$00D7	Port S Data Direction Register (DDRS) See page 222.	Read:	DDS7	DDS6	DDS5	DDS4	DDS3	DDS2	DDS1	DDS0
		Write:								
		Reset:	After reset all bits configured as general-purpose inputs							
$00D8	Reserved		R	R	R	R	R	R	R	R
↓										
$00DA	Reserved		R	R	R	R	R	R	R	R
$00DB	Port S Pullup/Reduced Drive Register (PURDS) See page 223.	Read:	0	RDPS2	RDPS1	RDPS0	0	PUPS2	PUPS1	PUPS0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00DC	Reserved		R	R	R	R	R	R	R	R
↓										
$00DF	Reserved		R	R	R	R	R	R	R	R

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Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 14 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$00E0	Slow Mode Divider Register (SLOW) See page 123.	Read:	0	0	0	0	0	SLDV2	SLDV1	SLDV0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00E1	Reserved		R	R	R	R	R	R	R	R
↓										
$00EF	Reserved		R	R	R	R	R	R	R	R
$00F0	EEPROM Configuration Register (EEMCR) See page 99.	Read:	1	1	1	1	1	EESWAI	PROTLCK	EERC
		Write:								
		Reset:	1	1	1	1	1	1	0	0
$00F1	EEPROM Block Protect Register (EEPROT) See page 100.	Read:	1	1	1	BRPROT4	BRPROT3	BRPROT2	BRPROT1	BRPROT0
		Write:								
		Reset:	1	1	1	1	1	1	1	1
$00F2	EEPROM Test Register (EETST) See page 101.	Read:	EEODD	EEVEN	MARG	EECPD	EECPRD	0	EECPM	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00F3	EEPROM Control Register (EEPROG) See page 102.	Read:	BULKP	0	0	BYTE	ROW	ERASE	EELAT	EEPGM
		Write:								
		Reset:	1	0	0	0	0	0	0	0
$00F4	FLASH EEPROM Lock Control Register (FEELCK)(1) See page 106.	Read:	0	0	0	0	0	0	0	LOCK
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00F5	FLASH EEPROM Configuration Register (FEEMCR)(1) See page 106.	Read:	0	0	0	0	0	0	0	BOOTP
		Write:								
		Reset:	0	0	0	0	0	0	0	1
$00F6	FLASH EEPROM Test Register (FEETST)(1) See page 107.	Read:	FSTE	GADR	HVT	FENLV	FDISVFP	VTCK	STRE	MWPR
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00F7	FLASH EEPROM Control Register (FEECTL)(1) See page 108.	Read:	0	0	0	FEESWAI	SVFP	ERAS	LAT	ENPE
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$00F8	BDLC Control Register 1 (BCR1)(2) See page 249.	Read:	IMSG	CLKS	R1	R0	0	0	IE	WCM
		Write:					R	R		
		Reset:	1	1	1	0	0	0	0	0
$00F9	BDLC State Vector Register (BSVR)(2) See page 256.	Read:	0	0	I3	I2	I1	I0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 15 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$00FA	BDLC Control Register 2 (BCR2)(2) See page 250.	Read: Write:	ALOOP	DLOOP	RX4XE	NBFS	TEOD	TSIFR	TMIFR1	TMIFR0
		Reset:	1	1	0	0	0	0	0	0
$00FB	BDLC Data Register (BDR)(2) See page 258.	Read: Write:	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
		Reset:	Indeterminate after reset							
$00FC	BDLC Analog Roundtrip Delay Register (BARD)(2) See page 259.	Read: Write:	ATE	RXPOL	0	0	BO3	BO2	BO1	BO0
		Reset:	1	1	0	0	0	1	1	1
$00FD	Port DLC Control Register (DLCSCR)(2) See page 260.	Read: Write:	0	0	0	0	0	BDLCEN	PUPDLC	RDPDLC
		Reset:	0	0	0	0	0	0	0	0
$00FE	Port DLC Data Register (PORTDLC)(2) See page 261.	Read: Write:	0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Reset:	0	U	U	U	U	U	U	U
$00FF	Port DLC Data Direction Register (DDRDLC)(2) See page 262.	Read: Write:	0	DDDLC6	DDDLC5	DDDLC4	DDDLC3	DDDLC2	DDDLC1	DDDLC0
		Reset:	0	0	0	0	0	0	0	0
$0100	msCAN12 Module Control Register 0 (CMCR0)(3) See page 284.	Read: Write:	0	0	CSWAI	SYNCH	TLNKEN	SLPAK	SLPRQ	SFTRES
		Reset:	0	0	1	0	0	0	0	1
$0101	msCAN12 Module Control Register 1 (CMCR1)(3) See page 286.	Read: Write:	0	0	0	0	0	LOOPB	WUPM	CLKSRC
		Reset:	0	0	0	0	0	0	0	0
$0102	msCAN12 Bus Timing Register 0 (CBTR0)(3) See page 287.	Read: Write:	SJW1	SJW0	BRP5	BRP4	BPR3	BPR2	BPR1	BPR0
		Reset:	0	0	0	0	0	0	0	0
$0103	msCAN12 Bus Timing Register 1 (CBTR1)(3) See page 288.	Read: Write:	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		Reset:	0	0	0	0	0	0	0	0
$0104	msCAN12 Receiver Flag Register (CRFLG)(3) See page 289.	Read: Write:	WUPIF	RWRNIF	TWRNIF	RERRIF	TERRIF	BOFFIF	OVRIF	RXF
		Reset:	0	0	0	0	0	0	0	0
$0105	msCAN12 Receiver Interrupt Enable Register (CRIER)(3) See page 291.	Read: Write:	WUPIE	RWRNIE	TWRNIE	RERRIE	TERRIE	BOFFIE	OVRIE	RXFIE
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 16 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0106	msCAN12 Transmitter Flag Register (CTFLG)(3) See page 292.	Read:	0	ABTAK2	ABTAK1	ABTAK0	0	TXE2	TXE1	TXE0
		Write:								
		Reset:	0	0	0	0	0	1	1	1
$0107	msCAN12 Transmitter Control Register (CTCR)(3) See page 293.	Read:	0	ABTRQ2	ABTRQ1	ABTRQ0	0	TXEIE2	TXEIE1	TXEIE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0108	msCAN12 Identifier Acceptance Control Register (CIDAC)(3) See page 294.	Read:	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0109	Reserved		R	R	R	R	R	R	R	R
↓										
$010D	Reserved		R	R	R	R	R	R	R	R
$010E	msCAN12 Receive Error Counter (CRXERR)(3) See page 295.	Read:	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$010F	msCAN12 Transmit Error Counter (CTXERR)(3) See page 295.	Read:	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0110	msCAN12 Identifier Acceptance Register 0 (CIDAR0)(3) See page 296.	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
		Reset:	Unaffected by reset							
$0111	msCAN12 Identifier Acceptance Register 1 (CIDAR1)(3) See page 296.	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
		Reset:	Unaffected by reset							
$0112	msCAN12 Identifier Acceptance Register 2 (CIDAR2)(3) See page 296.	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
		Reset:	Unaffected by reset							
$0113	msCAN12 Identifier Acceptance Register 3 (CIDAR3)(3) See page 296.	Read:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Write:								
		Reset:	Unaffected by reset							
$0114	msCAN12 Identifier Mask Register 0 (CIDMR0)(3) See page 297.	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
		Reset:	Unaffected by reset							
$0115	msCAN12 Identifier Mask Register 1 (CIDMR1)(3) See page 297.	Read:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Write:								
		Reset:	Unaffected by reset							

= Unimplemented R = Reserved U = Unaffected

Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 17 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0116	msCAN12 Identifier Mask Register 2 (CIDMR2)(3) See page 297.	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Reset:	Unaffected by reset							
$0117	msCAN12 Identifier Mask Register 3 (CIDMR3)(3) See page 297.	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Reset:	Unaffected by reset							
$0118	msCAN12 Identifier Acceptance Register 4 (CIDAR4)(3) See page 296.	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Reset:	Unaffected by reset							
$0119	msCAN12 Identifier Acceptance Register 5 (CIDAR5)(3) See page 296.	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Reset:	Unaffected by reset							
$011A	msCAN12 Identifier Acceptance Register 6 (CIDAR6)(3) See page 296.	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Reset:	Unaffected by reset							
$011B	msCAN12 Identifier Acceptance Register 7 (CIDAR7)(3) See page 296.	Read: Write:	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		Reset:	Unaffected by reset							
$011C	msCAN12 Identifier Mask Register 4 (CIDMR4)(3) See page 298.	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Reset:	Unaffected by reset							
$011D	msCAN12 Identifier Mask Register 5 (CIDMR5)(3) See page 298.	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Reset:	Unaffected by reset							
$011E	msCAN12 Identifier Mask Register 6 (CIDMR6)(3) See page 298.	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Reset:	Unaffected by reset							
$011F	msCAN12 Identifier Mask Register 7 (CIDMR7)(3) See page 298.	Read: Write:	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		Reset:	Unaffected by reset							
$0120	Reserved		R	R	R	R	R	R	R	R
↓										
$013C	Reserved		R	R	R	R	R	R	R	R
$013D	msCAN12 Port CAN Control Register (PCTLCAN)(3) See page 299.	Read:	0	0	0	0	0	0	PUECAN	RDPCAN
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 18 of 19)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$013E	msCAN12 Port CAN Data Register (PORTCAN)(3) See page 299.	Read:	PCAN7	PCAN6	PCAN5	PCAN4	PCAN2	PCAN2	TxCAN	RxCAN
		Write:								
		Reset:	Unaffected by reset							
$013F	msCAN12 Port CAN Data Direction Register (DDRCAN)(3) See page 300.	Read:	DDRCAN7	DDRCAN6	DDRCAN5	DDRCAN4	DDRCAN3	DDRCAN2	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0140 ↓ $014F	RECEIVE BUFFER (RxFG)(3) — SEE 16.3.2 Receive Structures									
$0150 ↓ $015F	TRANSMIT BUFFER 0 (Tx0)(3) — SEE 16.3.3 Transmit Structures									
$0160 ↓ $016F	TRANSMIT BUFFER 1 (TX1)(3) — SEE 16.3.3 Transmit Structures									
$0170 ↓ $017F	TRANSMIT BUFFER 2 (Tx2)(3) — SEE 16.3.3 Transmit Structures									

= Unimplemented R = Reserved U = Unaffected

Notes:
1. Available only on MC68HC912B32 and MC68HC912BC32 devices.
2. Available only on MC68HC912B32 and MC68HC12BE32 devices.
3. Available only on MC68HC(9)12BC32 devices.

Figure 2-1. Register Map (Sheet 19 of 19)