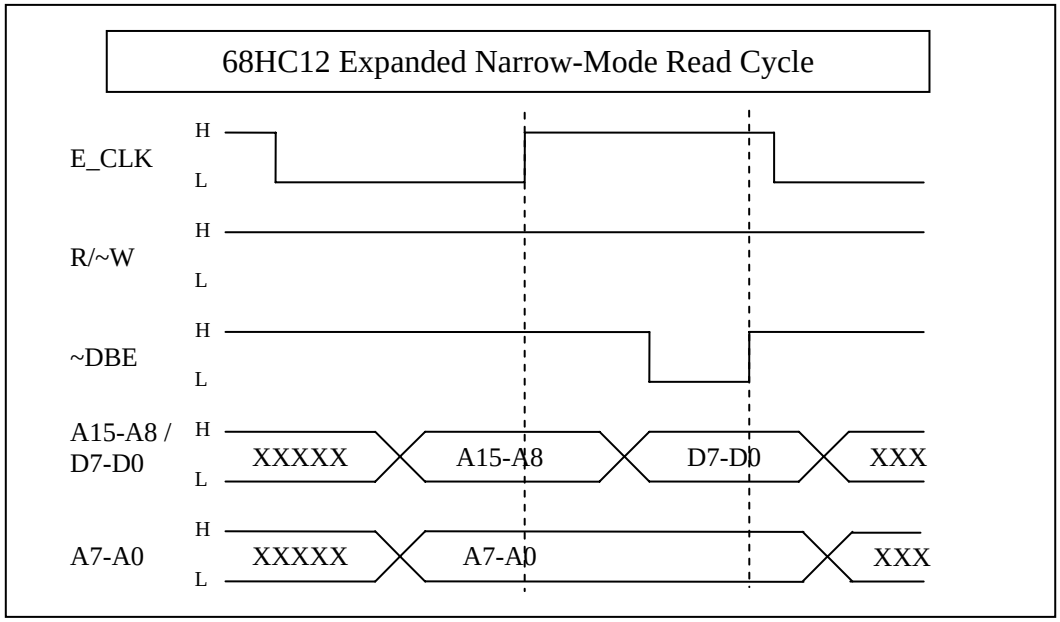
Simplified 68HC12 Expanded Narrow Mode Timing Diagrams

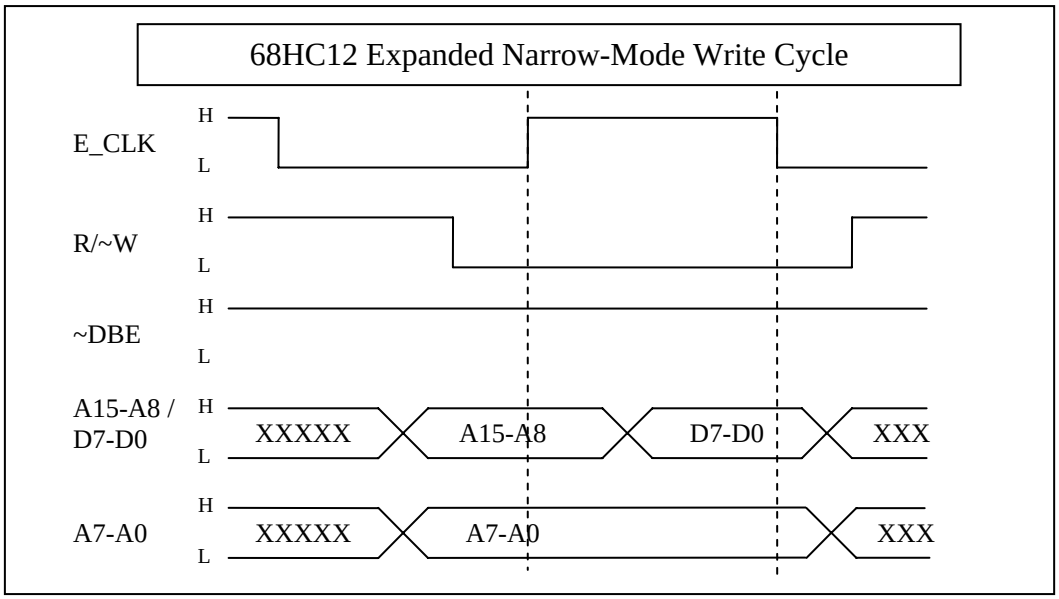
Summary on Expansion

- In narrow mode, A15-A8 pins are used for D7-D0.
- High address bits (A15:A8) are available at rising edge of E.
- Low address bits (A7:0) are **available when needed**, i.e., **no latch** is needed.
- Output data should be read while E is high and when R/~W is low.
- Input data is read on the rising edge of DBE when R/~W is high.
- An external latching device that receives output data from a 6812 write should start reading the data when R/~W is low and E goes high, but should not stop until the falling edge of E. If a synchronous device is used, the data should be read at the falling edge of E when R/~W low.
- An external device that sends input data for the 6812 to read should starts the process of outputting data when R/~W is high and DBE goes low (true). The input data is read on the rising edge of DBE.

For the UF 68HC12 board of Summer 2003

- Do to ringing of R/~W when it goes low, all address decoding for writes should include the E_CLK. (See document *RW_Ringing.pdf*, also available on the web.)





See M68HC12B/D, section 19.16 for more info

Below data is for a 4MHz oscillator ⇒ f_{E_CLK} = 2MHz and T_{E_CLK} = 500ns

READ (E_CLK=500ns)\

1. Addr setup time from E_CLK rise: 94ns (min)
2. Addr hold time E_CLK rise: 107ns (min)
3. Data setup from ECLK fall: 25ns (min)
4. Data hold time from E_CLK fall: 0ns (no need)
5. DBE delay time from E_CLK rise: 133ns (max)
6. DBE valid: 115ns (min)
7. DBE hold time to E_CLK fall: -10ns to 3ns

WRITE (E_CLK=500ns)\

1. Addr setup time from E_CLK rise: 94ns (min)
2. Addr hold time E_CLK rise: 107ns (min)
3. Data setup from ECLK fall: 83ns (min)
4. Data hold time from E_CLK fall: 20ns (min)