Pseudo-vector and vectors for the UF's 68HC12 board with our 68HC12 Monitor

Pseudo-Vector Address	Interrupt Pseudo-Vector Description
$0809-$080B	Analog-to-Digital Converter
$080C-$080E	Serial Communications Interface (SCI)
$080F-$0811	Serial Peripheral Interface (SPI)
$0812-$0814	Pulse Accumulator Input Edge
$0815-$0817	Pulse Accumulator Overflow
$0818-$081A	Timer Overflow
$081B-$081D	Timer Channel 7
$081E-$0820	Timer Channel 6
$0821-$0823	Timer Channel 5
$0824-$0826	Timer Channel 4
$0827-$0829	Timer Channel 3
$082A-$082C	Timer Channel 2
$082D-$082F	Timer Channel 1
$0830-$0832	Timer Channel 0
$0833-$0835	Real Time Interrupt (RTI)
$0836-$0838	IRQ
$0839-$083B	XIRQ
*$FF6C	Software Interrupt (SWI)
$083F-$0841	Unimplemented Opcode Trap
$0842-$0844	COP Failure Reset
$0845-$0847	Clock Monitor Failure Reset
$0848-$084A	Reset
*$FF80	Reset

Vector Address	Interrupt Source	CCR Mask	Register	Bits	HPRIO Value to Elevate to Highest I Bit
$FFFE-$FFFF	Reset	None	None	None	---
$FFFC-$FFFD	Clock monitor fail reset	None	COPCTL	CME, FCME	---
$FFFA-$FFFB	COP failure reset	None	None	COP rate selected	---
$FFF8-$FFF9	Unimplemented instruction trap	None	None	None	---
$FFF6-$FFF7	SWI	None	None	None	---
$FFF4-$FFF5	XIRQ	X bit	None	None	---
$FFF2-$FFF3	IRQ	I bit	INTCR	IRQEN	$F2
$FFF0-$FFF1	Real Time Interrupt (RTI)	I bit	RTICTL	RTIE	$F0
$FFEE-$FFEF	Timer Channel 0	I bit	TMSK1	C0I	$EE
$FFEC-$FFED	Timer Channel 1	I bit	TMSK1	C1I	$EC
$FFEA-$FFEB	Timer Channel 2	I bit	TMSK1	C2I	$EA
$FFE8-$FFE9	Timer Channel 3	I bit	TMSK1	C3I	$E8
$FFE6-$FFE7	Timer Channel 4	I bit	TMSK1	C4I	$E6
$FFE4-$FFE5	Timer Channel 5	I bit	TMSK1	C5I	$E4
$FFE2-$FFE3	Timer Channel 6	I bit	TMSK1	C6I	$E2
$FFE0-$FFE1	Timer Channel 7	I bit	TMSK1	C7I	$E0
$FFDE-$FFDF	Timer overflow	I bit	TMSK2	TO	$DE
$FFDC-$FFDD	Pulse accumulator overflow	I bit	PACTL	PAOVI	$DC
$FFDA-$FFDB	Pulse accumulator input edge	I bit	PACTL	PAI	$DA
$FFD8-$FFD9	SPI serial transfer complete	I bit	SP0CR1	SPIE	$D8
$FFD6-$FFD7	SCI0	I bit	SP0CR2	TIE, TCIE, RIE, ILIE	$D6
$FFD4-$FFD5	Reverved	I bit	---	---	$D4
$FFD2-$FFD3	ATD	I bit	ATDCTL2	ASCIE	$D2
$FFD0-$FFD1	MSCAN wakeup	I bit	CRIER	WUPIE	$D0
$FFCA-$FFCF	Reserved (not implemented)	I bit	---	---	$CA-CF
$FFC8-$FFC9	MSCAN errors	I bit	CRIER	*	$C8
$FFC6-$FFC7	MSCAN receive	I bit	CRIER	RXFIE	$C6
$FFC4-$FFC5	MSCAN transmit	I bit	CTCR	TXEIE[2:0}	$C4
$FF80-$FFC3	Reserved (implemented)	I bit	---	---	$80-$C3

* = RWRNIE, TWRNIE, RERRIE, TERRIE, BOFFIE, OVRIE