

out of the **B** **X**

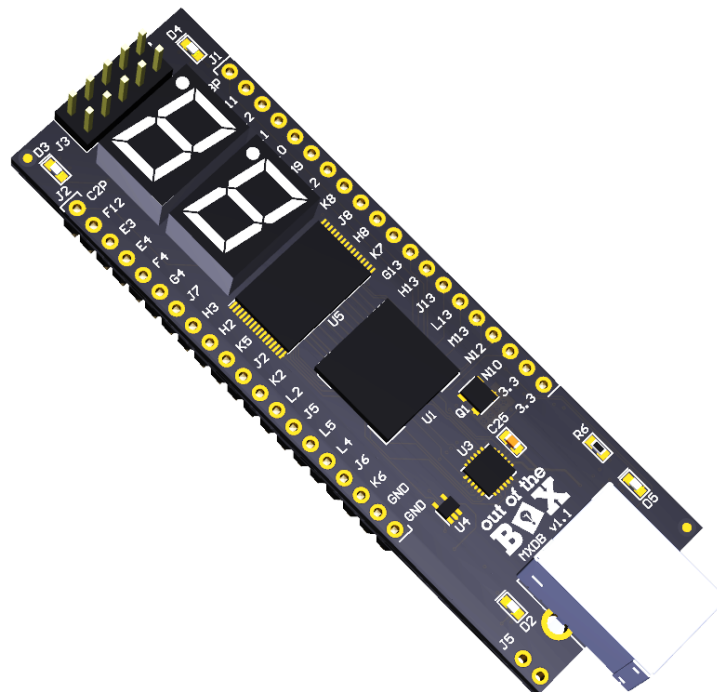
MXDB

MAX 10 Development Board

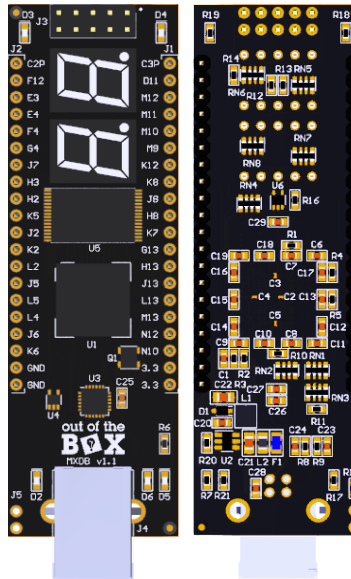
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Overview



The MXDB is Out of the Box's 2nd generation programmable logic development platform. The MXDB is a platform designed specifically for learning the basics of digital electronics from the lowest level of logic gates to microprocessors. The board features a USB FIFO bridge, external flash memory and accompaniment software to program data to the flash memory with a PC. The board's form-factor also makes it ideal for interfacing with a solderless breadboard.

Warning Read Before Continuing

The MXDB is a FPGA platform that also contains additional ICs capable of driving signals to the FPGA controlled via read strobe pins. There is a jumper **J5** that when left open will help prevent inadvertent IO conflicts, but this should not be considered a complete solution! It is the user's responsibility to review the device schematic and the FPGA pin planner assignments before uploading any design to the device.

Features

MAX 10 CPLD

The MXDB is by default configured with a MAX 10 2K logic element FPGA. Unlike most FPGAs the MAX 10 has built in non-volatile memory allowing the device to function like a CPLD.

I/O and Indicators

The MXDB has 34 GPIO pins 2 of which are optionally used a global clock inputs. There are also 4 general purpose LEDs, 2 seven segment LED displays, and a single power LED.

USB

The MXDB is equipped with a FT-240X USB to FIFO bridge that allows the FPGA to send and receive data from a PC USB connection. This device is utilized for the Out of the Box Flash Programmer GUI, used to program the on-board parallel flash IC.

External Flash Memory

The MXDB features parallel flash memory connected to the FPGA. This ROM could be used for simple look up tables, soft processor program memory etc.

USB Flash Programming

As mentioned above the Out of the Box Flash Programmer GUI interfaces with the MXDB's USB connection in order to program to and read from the on-board flash memory.

IO Protection

The MXDB has a jumper **J5** used to allow the use of the read strobe signals to the USB to FIFO device and the parallel flash. With this jumper open the read strobes will be pulled false. This jumper is used to **help prevent** bus conflicts if an inexperienced user accidentally assigns a design pin to a strobe erroneously. Doing so could allow the flash or USB devices to drive pins to the FPGA.

Note: to utilize the flash Programmer GUI this jumper must be present.

Electrical Characteristics

Electrical Characteristics

Item	Min	Nominal	Max	Unit
Un-programmed Current draw	< 20			mA
3.3V current output ¹²		~700 ²	1500 ²	mA
GPIO VIH			3.6	V
GPIO VIL	-0.3		0.8	V

- 1) This includes the current required to power the board itself
- 2) The current output is likely limited by efficiency of the regulator and maximum current of USB 2.0 (500mA). The 3.3V regulator is rated for 1.5A output.