

### Timer/Counter1 Control Register A – TCCR1A

Bit	7	6	5	4	3	2	1	0	
	<div style="border: 1px solid black; padding: 2px; display: inline-block;"> <span style="margin-right: 5px;">COM1A1</span> <span style="margin-right: 5px;">COM1A0</span> <span style="margin-right: 5px;">COM1B1</span> <span style="margin-right: 5px;">COM1B0</span> <span style="margin-right: 5px;">COM1C1</span> <span style="margin-right: 5px;">COM1C0</span> <span style="margin-right: 5px;">WGM11</span> <span style="margin-right: 5px;">WGM10</span> </div>								TCCR1A
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

### Timer/Counter1 Control Register B – TCCR1B

Bit	7	6	5	4	3	2	1	0	
	<div style="border: 1px solid black; padding: 2px; display: inline-block;"> <span style="margin-right: 5px;">ICNC1</span> <span style="margin-right: 5px;">ICES1</span> <span style="margin-right: 5px;">–</span> <span style="margin-right: 5px;">WGM13</span> <span style="margin-right: 5px;">WGM12</span> <span style="margin-right: 5px;">CS12</span> <span style="margin-right: 5px;">CS11</span> <span style="margin-right: 5px;">CS10</span> </div>								TCCR1B
Read/Write	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

**Table 60.** Compare Output Mode, Phase Correct and Phase and Frequency Correct PWM

COMnA1/COMnB1/ COMnC1	COMnA0/COMnB0/ COMnC0	Description
0	0	Normal port operation, OCnA/OCnB/OCnC disconnected.
0	1	WGMn3:0 = 9 or 11: Toggle OCnA on Compare Match, OCnB/OCnC disconnected (normal port operation). For all other WGMn settings, normal port operation, OCnA/OCnB/OCnC disconnected.
1	0	Clear OCnA/OCnB/OCnC on compare match when up-counting. Set OCnA/OCnB/OCnC on compare match when downcounting.
1	1	Set OCnA/OCnB/OCnC on compare match when up-counting. Clear OCnA/OCnB/OCnC on compare match when downcounting.

Note: A special case occurs when OCRnA/OCRnB/OCRnC equals TOP and COMnA1/COMnB1/COMnC1 is set. See “Phase Correct PWM Mode” on page 127. for more details.

**Table 61.** Waveform Generation Mode Bit Description

Mode	WGMn3	WGMn2 (CTCn)	WGMn1 (PWMn1)	WGMn0 (PWMn0)	Timer/Counter Mode of Operation <sup>(1)</sup>	TOP	Update of OCRnX at	TOVn Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, Phase Correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, Phase Correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, Phase Correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCRnA	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	BOTTOM	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	BOTTOM	TOP
8	1	0	0	0	PWM, Phase and Frequency Correct	ICRn	BOTTOM	BOTTOM
9	1	0	0	1	PWM, Phase and Frequency Correct	OCRnA	BOTTOM	BOTTOM
10	1	0	1	0	PWM, Phase Correct	ICRn	TOP	BOTTOM
11	1	0	1	1	PWM, Phase Correct	OCRnA	TOP	BOTTOM
12	1	1	0	0	CTC	ICRn	Immediate	MAX
13	1	1	0	1	(Reserved)	–	–	–
14	1	1	1	0	Fast PWM	ICRn	BOTTOM	TOP
15	1	1	1	1	Fast PWM	OCRnA	BOTTOM	TOP

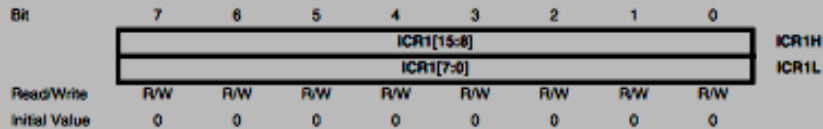
Note: 1. The CTCn and PWMn1:0 bit definition names are obsolete. Use the WGMn2:0 definitions. However, the functionality and location of these bits are compatible with previous versions of the timer.

**Table 62. Clock Select Bit Description**

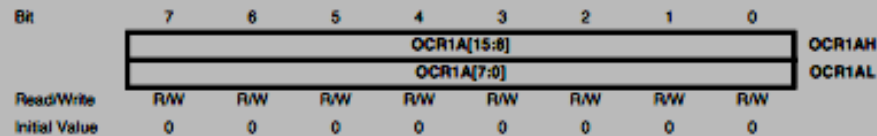
CSn2	CSn1	CSn0	Description
0	0	0	No clock source. (Timer/Counter stopped)
0	0	1	$clk_{IO}/1$ (No prescaling)
0	1	0	$clk_{IO}/8$ (From prescaler)
0	1	1	$clk_{IO}/64$ (From prescaler)
1	0	0	$clk_{IO}/256$ (From prescaler)
1	0	1	$clk_{IO}/1024$ (From prescaler)
1	1	0	External clock source on Tn pin. Clock on falling edge
1	1	1	External clock source on Tn pin. Clock on rising edge

If external pin modes are used for the Timer/Counter, transitions on the Tn pin will clock the counter even if the pin is configured as an output. This feature allows software control of the counting.

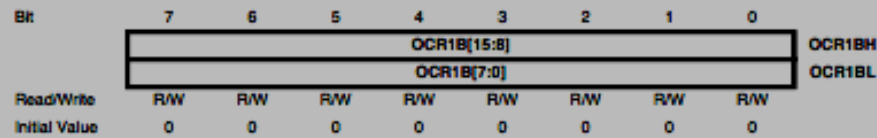
**Input Capture Register  
1 – ICR1H and ICR1L**



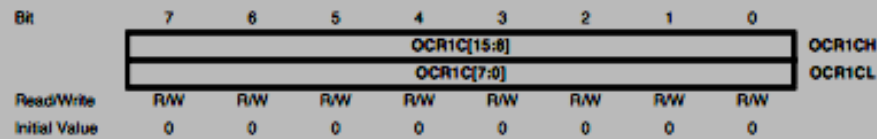
**Output Compare  
Register 1 A –  
OCR1AH and OCR1AL**



**Output Compare  
Register 1 B –  
OCR1BH and OCR1BL**



**Output Compare  
Register 1 C –  
OCR1CH and OCR1CL**



Similar configuration for Timer 3

For  $f=50\text{Hz}$  ( $T=20\text{ ms}$ ) servos in the ATmega128 we want:

**TCCR1A**

COM1A1	COM1A0	COM1B1	COM1B0	COM1C1	COM1C0	WGM11	WGM10
1	0	1	0	1	0	0	0

**TCCR1B**

ICNC1	ICES1	-	WGM13	WGM12	CS12	CS11	CS10
0	0	0	1	0	0	1	0

**ICR1 Input Capture Register 1 – ICR1H and ICR1L** **0x4E20=20,000**

7	6	5	4	3	2	1	0
0	1	0	0	1	1	0	0
0	0	1	0	0	0	0	0

ICR1H

ICR1L

**OCR1A Output Compare Register 1A – OCR1AH and OCR1AL** **0x05DC= 1,500**

7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1
1	1	0	1	1	1	0	0

OCR1AH

OCR1AL

**OCR1B Output Compare Register 1B – OCR1BH and OCR1BL** **0x05DC= 1,500**

7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1
1	1	0	1	1	1	0	0

OCR1AH

OCR1AL

**OCR1C Output Compare Register 1C – OCR1CH and OCR1CL** **0x05DC= 1,500**

7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	1
1	1	0	1	1	1	0	0

OCR1AH

OCR1AL

OC1A ≡ PB5

OC1B ≡ PB6

OC1C ≡ PB7

OC3A ≡ PE3

OC3B ≡ PE4

OC3C ≡ PE5