GuP: Configuration ROM

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The **EPCS4** is a ROM (flash) used to retain the configuration of an Altera FPGA like the ones used on the GuP main board and on the GuP expansion board. The **EPCS4** is programmed in **Active Serial Programming** mode.

The below information is taken from the Quartus II Version 8.0 Handbook, Volume 3, Section VII, Chapter 19. Quartus II Programmer (see http://www.altera.com/literature/lit-qts.jsp to download the entire manual or sections, see http://www.altera.com/literature/hb/qts/quartusii_handbook.pdf for the entire manual, see http://www.altera.com/literature/hb/qts/qts_qii5v3_07.pdf for the Chapter 19 information discussed below (from pages 1-5 in Chapter 19).

For details about programming devices and creating secondary programming files, see subsection *Programming & Configuration Modes of Chapter 19: Quartus II Programmer* in the *Quartus II Version 8.0 Handbook, Volume 3, Section VII*.

Use JTAG programming mode to directly program the FPGA. Note that the program will not survive a power reset.

*Check out the Quartus II tutorials found under the Help menu.

EPCS4 is referred to as both a “serial configuration device” and an “enhanced configuration device”.

Table 19–1. Programming and Configuration File Format

File Format	FPGA	CPLD	Configuration Device and Enhanced Configuration Device	Serial Configuration Device
SRAM Object File (**.sof**)	✓	—	—	—
Programmer Object File (**.pof**)	—	✓	✓	✓
Jam File (**.jam**)	✓	✓	✓	—
Jam Byte-Code File (**.jbc**)	✓	✓	✓	—

Table 19-1 from *Chapter 19. Quartus II Programmer*

ACTIVE SERIAL MODE

You can use the active serial (AS) mode to program serial configuration devices. After programming completes, the serial configuration device then configures the FPGA. AS programming uses the DATA, DCLK, nCS, and ASDI pins. If the download cable is connected to the nCONFIG and nCE pins of the FPGA, the download cable disables the FPGA’s access to the AS interface by holding the nCE pin high and the nCONFIG pin low. Upon completion of the programming, the nCE and nCONFIG pins are released and the FPGA configuration begins.

For more information about programming the serial configuration device, configuring the FPGA with the serial configuration device through AS mode, or the AS pin connection, refer to the Serial Configuration Data Sheet in the Configuration Handbook (see the file at http://www.altera.com/literature/hb/cfg/config_handbook.pdf) or the chapter on configuration in the appropriate FPGA device handbook.

Table 19–2. Programming and Configuration Modes

Mode	FPGA	CPLD	Configuration Device and Enhanced Configuration Device	Serial Configuration Device
JTAG	✓	✓	✓	—
PS	✓	—	—	—
AS	—	—	—	✓
In-Socket Programming	—	✓(1)	✓	✓

Table 19-2 from *Chapter 19. Quartus II Programmer*

INSTRUCTIONS FOR PROGRAMMING THE EPCS4

The EPCS4 configuration ROM enables the FPGA configuration to persist through multiple power resets. Screen shots follow the written instructions.

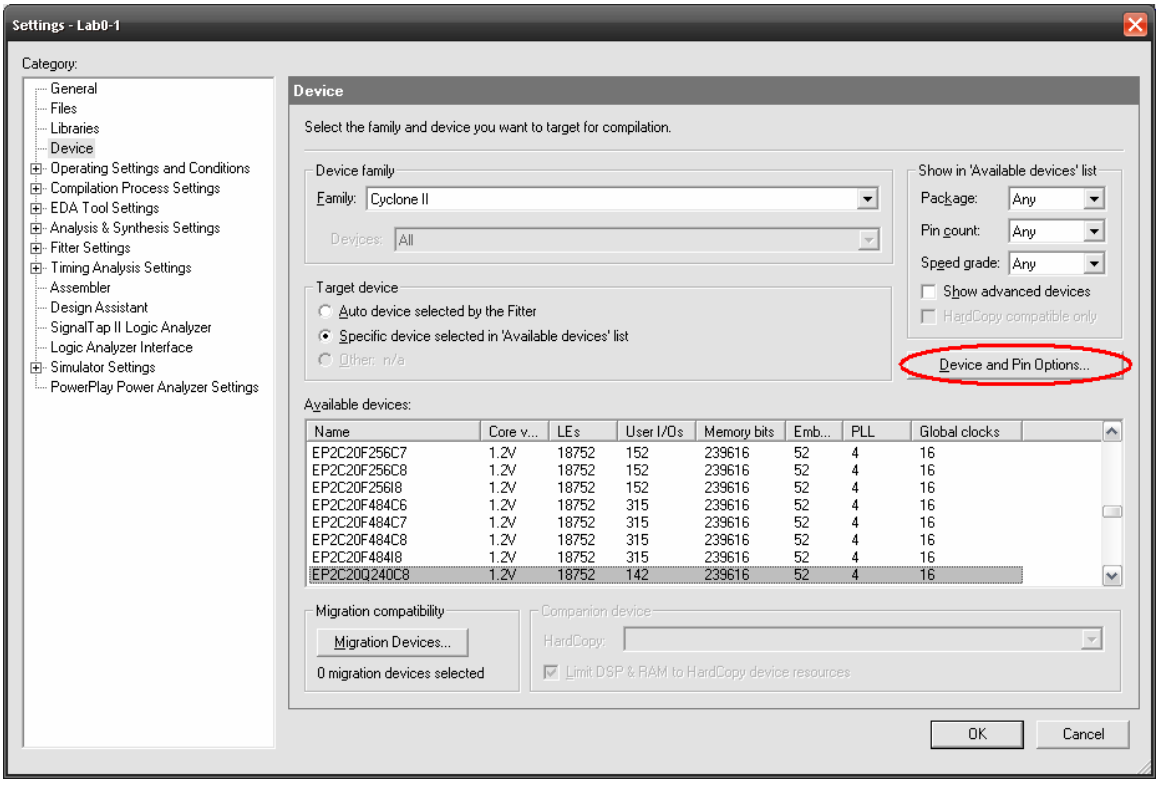
There is an EPCS4 available on the GuP main board (optional for 4712 students) and a required EPCS4 on the GuP expansion board used exclusively for EEL4744. The EPCS4 on the main board is also required for EEL 4744 students. There is a jumper on the main board in the lower left hand corner that must be set appropriately to program one or the other configuration devices. The two jumper selection options are labeled INT or EXP (expansion). Select INT to program the EPCS4 on the main board and EXP to program the EPCS4 on the expansion board.

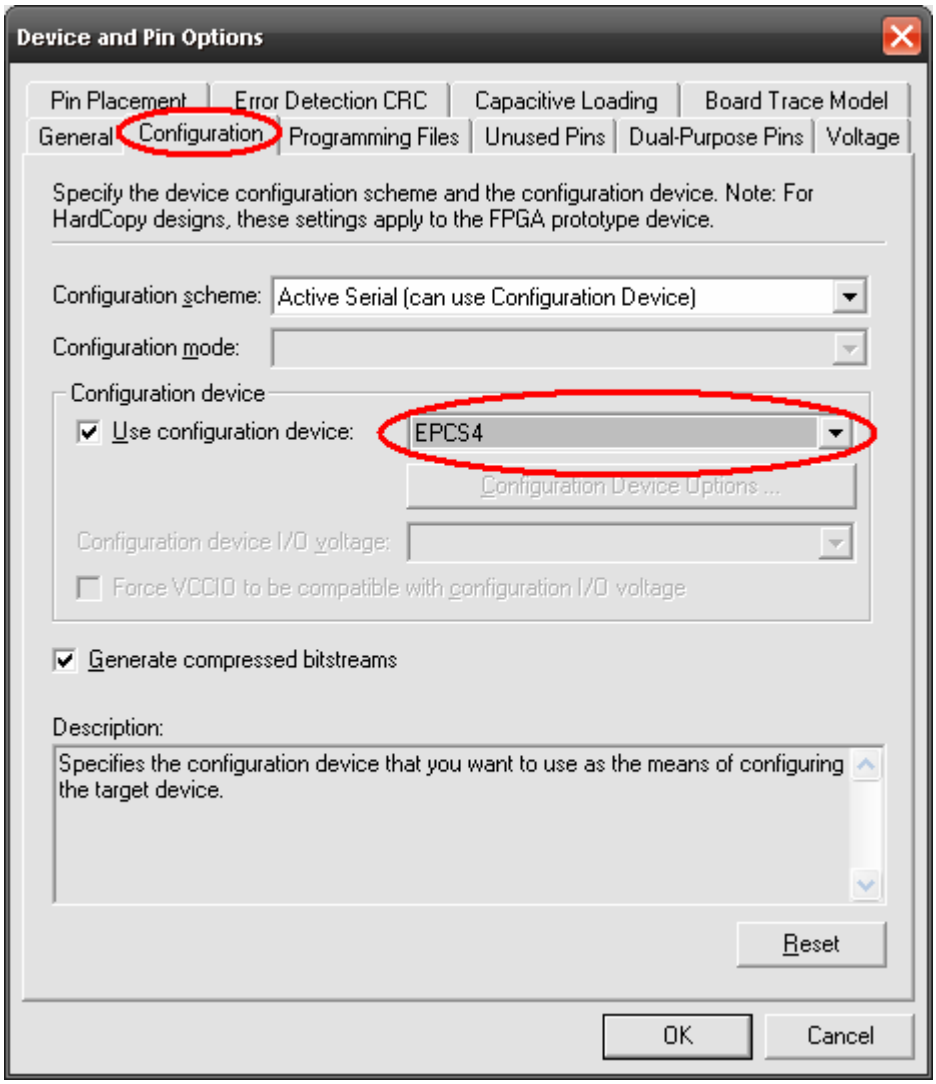
Use the header labeled “ISP Port” to program the selected EPCS4 configuration ROM. Both configuration ROM’s are preloaded with the latest version of the GuP.

EEL 4744 students will want to store the changes you make in Quartus on the configuration ROM on the expansion board whenever you change the address decoding. The expansion board configuration ROM is actually optional and will not be pre-installed when the board goes into full production.

To program the configuration ROM, in Quartus, go to “Assignment | Device…” and after selecting your correct device (FPGA), click on the “Device and Pin Options…” button, “Configuration” tab, and under “Configuration device” select the EPCS4. Click OK to get out of all the windows and fully compile the project.

Connect the USB Blaster cable to the ISP port on your board. Go to the Programmer app in Quartus, use “Active Serial Programming” as your mode, select the .pof corresponding to your project and select the “Program/Configure” and “Verify” options. Click Start and in about 15 seconds the operation is complete.


Settings - Lab0-1
Category:
General
Files
Libraries
Device
Operating Settings and Conditions
Compilation Process Settings
EDA Tool Settings
Analysis & Synthesis Settings
Fitter Settings
Timing Analysis Settings
Assembler
Design Assistant
SignalTap II Logic Analyzer
Logic Analyzer Interface
Simulator Settings
PowerPlay Power Analyzer Settings
Device
Select the family and device you want to target for compilation.
Device family
Family: Cyclone II
Devices: All
Target device
Auto device selected by the Fitter
Specific device selected in 'Available devices' list
Other: n/a
Show in 'Available devices' list
Package: Any
Pin count: Any
Speed grade: Any
Show advanced devices
HardCopy compatible only
Device and Pin Options...
Available devices:
Name Core v... LEs User I/Os Memory bits Emb... PLL Global clocks
EP2C20F256C7 1.2V 18752 152 239616 52 4 16
EP2C20F256C8 1.2V 18752 152 239616 52 4 16
EP2C20F256I8 1.2V 18752 152 239616 52 4 16
EP2C20F484C6 1.2V 18752 315 239616 52 4 16
EP2C20F484C7 1.2V 18752 315 239616 52 4 16
EP2C20F484C8 1.2V 18752 315 239616 52 4 16
EP2C20F484I8 1.2V 18752 315 239616 52 4 16
EP2C20Q240C8 1.2V 18752 142 239616 52 4 16
Migration compatibility
Migration Devices...
0 migration devices selected
Companion device
HardCopy:
Limit DSP & RAM to HardCopy device resources
OK
Cancel


Device and Pin Options
Pin Placement
Error Detection CRC
Capacitive Loading
Board Trace Model
General
Configuration
Programming Files
Unused Pins
Dual-Purpose Pins
Voltage
Specify the device configuration scheme and the configuration device. Note: For HardCopy designs, these settings apply to the FPGA prototype device.
Configuration scheme:
Active Serial (can use Configuration Device)
Configuration mode:
Configuration device
Use configuration device:
EPCS4
Configuration Device Options ...
Configuration device I/O voltage:
Force VCCIO to be compatible with configuration I/O voltage
Generate compressed bitstreams
Description:
Specifies the configuration device that you want to use as the means of configuring the target device.
Reset
OK
Cancel