

STEP-DOWN SWITCHING REGULATOR LIGHT-LOAD EFFICIENCY  
IMPROVEMENT USING RECYCLED PARASITIC ENERGY, AND GATE  
VOLTAGE CLAMPING

By

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Abstract{ TC "ABSTRACT" } of Thesis Presented to the Graduate School  
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An energy efficient gate drive method is provided for switching on and off field effect transistors (FET) arranged in a binary push-pull configuration having a common center switch-node. Current methods waste parasitic energy stored in parasitic capacitive and inductive elements. One aspect of the present method recycles some of this otherwise lost parasitic energy at the switch-node to turn on the push-pull FETs. As applied to step-down switch-mode voltage regulators, the switch-node is further used to increase switching efficiency by timing a low voltage gate drive process, thereby resulting in a significantly improved noise and efficiency performance under light-loads and high input voltages. A method for detecting a light-load condition by sensing a load dependant zero-crossing voltage at the switch-node is also provided.

## CHAPTER 1 INTRODUCTION

### **Scope**

The present Thesis relates generally to switching DC-DC regulators, and more particularly, to fixed frequency switching DC-DC regulators that maintain high light-load efficiency when using large external FET switching devices. The scope includes methods to configure the gate drive of binary, push-pull arranged MOSFETs for increased switching efficiency, a method to detect light-loads, and a synchronous buck regulator design implementing these methods.

### **Organization**

The present paper is arranged to initially provide a high-level overview of the novel methods presented. Synchronous buck regulator architectures are well-known to those in the art. Hence, a basic buck regulator background is presented that focuses on aspects important to the concepts introduced herein. These concepts are initially explored by way of a survey of the closest known art.

There are three principle technologies introduced: recycled gate drive energy, light-load detection, and a low-voltage gate drive scheme. Each novel method is introduced by describing the basic approach, followed by implementation details, results (if any), and a summary conclusion. The foregoing technologies are applied to a synchronous buck regulation system to improve power efficiency, especially at light-loads. Implementation details and simulation results are presented.

## **Methodology**

The results presented in this paper are supported by way of theoretical discourse, and simulation results. Details have been omitted when well known to those in the art of electronics and switching regulator design. Principally, simulation results are relied upon to validate design performance. Results are generated by a generic XSPICE simulator that accepts standard PSPICE models of components such as the power MOSFETs used.

## CHAPTER 2 EXECUTIVE SUMMARY

This Thesis discovers novel methods to significantly improve the switch efficiency of binary push-pull configured metal oxide semiconductor field effect transistors (MOSFETs), while not significantly increasing system cost or complexity. In particular, the goal is to improve the efficiency of a synchronous step-down DC-DC switching regulator design known as a “buck” regulator. The buck regulator has a pair of output power MOSFETs arranged in the push-pull topology having a common switch-node. It is well known to those in the art of digital design that the energy transfer efficiency of switching MOSFETs on and off is dominated by the supply voltage, switching frequency, and MOSFET gate capacitance. By addressing each factor, the presented methods increase power conversion efficiency when any combination of the following is true: the output loading current is low, the switching frequency is high, the MOSFET gate capacitance is large, and/or the input voltage is high. The poor efficiency problem dramatically increases at light-loads because much more power is lost by switching on and off large power MOSFET switches than that lost to DC conduction losses due to the MOSFET’s conduction resistance.

The present design uses energy and voltages from the common switch-node of the output MOSFETs to turn on the appropriate output MOSFET in a very efficient manner. The gate drive signals that turn on and off the output MOSFETs are similar to known methods; however, the amplitudes of the gate drive voltages have been reduced to the

respective minimal voltage required to fully turn on each output MOSFET, thereby decreasing the amount of energy wasted in toggling there state each switching period. Additionally, much of the energy required to turn on each output MOSFET is derived from the switch-node, instead of the power supply as in known approaches. From a functional point of view, the present design behaves similar to known buck switching regulators. Notably, the switching elements that turn off the output MOSFETs are connected as in standard techniques. By providing a controlled path between the switch-node and each output MOSFET gate, energy stored in storage elements at the switch-node can be directed to turn on each MOSFET at the correct time.

Several methods are provided to recycle switch-node energy, and set the gate drive voltage to a low value. Techniques presented include diode clamping and MOSFET clamping. In diode clamping, a diode voltage drop is used to force the output MOSFET gate voltage to a predefined voltage level. In MOSFET clamping, a reference voltage source is applied to the gate of a clamping MOSFET whereby the output MOSFET's gate voltage is forced to be near the reference voltage applied to the clamping MOSFET. The clamping MOSFET pulls the output MOSFET's gate voltage towards the reference voltage until the clamping MOSFET turns off as the difference between the reference voltage applied to its gate and output MOSFET's gate voltage becomes less than the turn-on threshold voltage of the clamping MOSFET.

A further exploit of the switch-node enables a more simple and cost effective way to detect when a light-load condition exists, and thereby when the specialized gate drive circuits of the present design should be used. Known methods insert an inline load-current sensing resistor in the output, load-current path to detect when the output load-

current is low enough to benefit from engaging various known energy saving measures. Importantly, the present method does not require a sensing resistor that increases cost, and decreases efficiency. Instead, a mode known as a “discontinuous mode” is used to signal the light-load switch point. The discontinuous mode occurs when a triangular shaped switching current in the switching regulator’s inductor runs out of energy and dips below ground potential. The average level of the inductor current is equal to the output load-current. In this way, the onset of the discontinuous mode can be designed to occur at a desired load-current value by selecting an appropriate inductor value. Detection of the discontinuous mode is achieved at the switch-node that is connected to the inductor. A positive-going switch-node voltage induced during discontinuous mode operation is used to sense the light-load condition.

## CHAPTER 3 BACKGROUND

### **Basic Synchronous Buck Regulator Theory of Operation**

To appreciate the implementation and benefits of the present approach a brief discussion of the basic synchronous buck switch-mode voltage regulator follows. A standard synchronous buck regulator is shown in Figure 3-1 with the gate drive circuit depicted as a functional block. It is referred to as “synchronous” because transistor **Q1** is present where as a “non-synchronous” buck regulator uses a simple diode, such as **D1**, instead. A synchronous regulator has the advantage of having a much lower DC power loss thereby resulting in much higher efficiency at moderate to high output load currents. Efficiency is worse at light-loads; however, because of the significantly higher switching losses than that of a diode. Using the same reasoning, a “non-synchronous” buck regulator has better light-load efficiency by virtue of lower switching losses and worse efficiency than a synchronous regulator as the output load-current rises. As will be described in more detail below, many applications that require low system noise values must operate in synchronous mode to avoid asynchronous power supply spikes, and tank circuit ring that occurs when the switch-node is floating as the output inductor current in **L1** is blocked by diode **D1**.

The regulation cycle begins with the gate drive circuit turning on the PMOS switch **Q1**, during what is referred to as “on-time,” to charge inductor **L1** and capacitor **C1**. After a predetermined period of “on-time” PMOS switch **Q1** is turned off and the NMOS switch **Q2** is turned on during what is referred to as “off-time” to circulated the

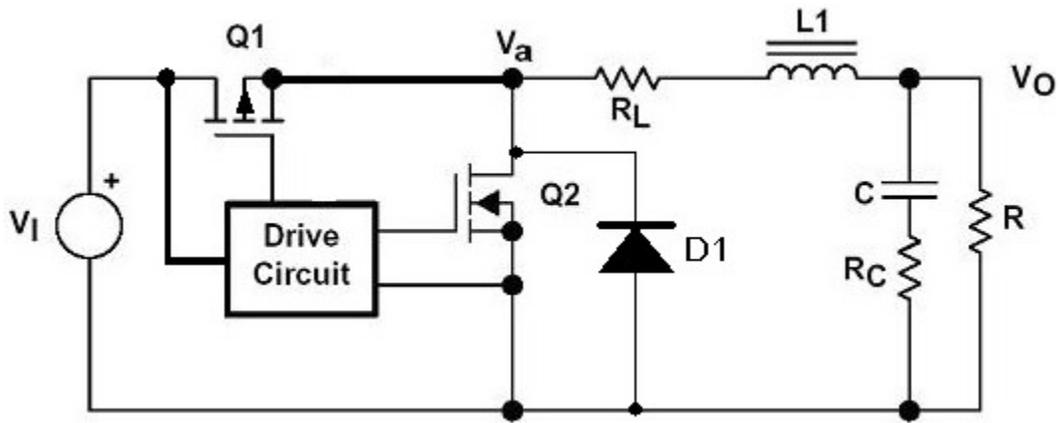


Figure 3-1<sup>1</sup> Basic Synchronous Buck circuit.

current stored in inductor **L1** to load **R**, thereby generating an output voltage **VO**. The common node **Va** shared by **Q1** and **Q2** is referred to as the switch-node. The alternation between on-time and off-time generates a push-pull square wave at switch-node **Va** that is filtered by the output filter formed by **L1**, **C**, **RL**, **RC** and **R**. As can be derived by the volt-second inductor equation  $V = L \, di/dt$ , the duration of the on-time, or duty cycle, is predominantly determined by the ratio of output voltage **VO** to input voltage **V1**. The duty cycle will increase from this ratio to compensate for energy lost to parasitic resistive components such as the conduction resistance in **Q1/Q2**, **RL**, and **RC**. A negative feedback voltage regulation control loop (not shown) is formed by feeding back **VO** to a comparator (not shown) in the drive circuit that compares **VO** against a periodic ramp voltage signal. If **VO** is below the ramp voltage then the gate drive circuit switches to on-time, and if below, off-time is triggered. In this way, the output voltage **VO** is regulated to a fix voltage, largely independent of variations in **V1** and the load-current.

Known synchronous buck regulators operate in three main modes referred to as continuous, discontinuous, and burst modes. At normal loads both **Q1** and **Q2** alternate

<sup>1</sup> Derived from Everett Rogers, Understanding Buck Power Stages in Switchmode Power Supplies, SLVA057, Texas Instruments Incorporated Inc. (Dallas, Texas, Mar. 1999), Figure 1, p. 2.

continuously to drive a square wave at switch-node  $V_a$  oscillating at the switching frequency (usually greater than 200KHz). At light-loads, however, discontinuous and burst modes are often employed to maintain high efficiency. In discontinuous mode, the off-time FET is disabled when  $L1$  is out of energy, whereby a characteristic high frequency, L-C-R tank circuit ringing oscillation results. Disabling the off-time FET improves light-load efficiency by using parallel diode  $D1$  to prevent  $L1$  from charging in the wrong direction, at the cost, however, of generating broad spectral noise resulting from L-C-R ringing when the switch-node is unconnected to ground.

The burst mode light-load efficiency boosting strategy skips switching periods and turns on with a predetermined number of burst only when  $V_O$  drops below a certain threshold, thereby randomly turning on when needed. At light-load, the switching power losses dominate, so the burst mode method seeks to minimize the switching frequency. The burst mode reduces switching frequency by skipping switching periods and passing more energy during each cycle of the multi-cycle burst sequence. This is useful only in cases that can tolerate high ripple and broad-spectrum noise. Unfortunately, the burst frequency is unpredictable in the range of zero to the switching frequency, and has been observed to routinely generate strong spectral energy in the audio and ultrasound range that significantly interferes with sensitive analog sensors such as the 40KHz analog IR sensor used on robots, ultrasound radar sensors, and many other frequency sensitive sensors. Thus, it is highly desirable to find a method to improve light-load efficiency whereby the buck regulator can operate efficiently, while not going into burst mode at light-load-currents.

To turn on the NMOS, and turn off the PMOS, known driver circuits apply charge from the power supply  $V_I$  to the gates of each FET. Similarly, to turn off the NMOS, and turn on the PMOS, known driver circuits remove charge from the gates of each FET by grounding them. In this way, a substantial amount of power is lost each time these FETs switch their conduction state, wherein this switching power loss is proportional to the FET gate capacitance. The basic variables in the power loss equation are the switching frequency/period ( $f_s$ )/( $T_s$ ), switch ON resistance ( $R_{dsON}$ ), load-current  $I$ , gate capacitance ( $C_g$ ), and gate-to-source voltage ( $V_{gs}$ ), where the power loss is given by Equation (1):

$$P_{loss} = 2C_g * V_{gs}^2 f_s + * \frac{R_{dsON} * I^2}{3T_s} \quad (1)$$

Hence, this switching power loss becomes dominant as the switching frequency increases, input voltage rises, the FETs become larger, and/or the load-current decrease. By way of example, observations and simulations indicate that a 1 MHz buck regulator capable of delivering 2 A load-current using output FETs having a 100 mOhm on resistance and a 10 V input voltage has an unacceptably low efficiency value of around .3% at a light-load of around 100mA. As a reference, a similar low power buck switching at 680 KHz, using 600 mOhm FETs capable of delivering around 200mA has an excellent efficiency value of about 92% at the same 100 mA light-load.

As a result of the extremely poor light-load efficiency of high power FETs, several desirable applications and production cost reductions are not possible. For example, it is desirable to increase the switching frequency  $f_s$ , as high as possible because a smaller inductor  $L1$  and capacitor  $C1$  can achieve the same electrical performance, thereby reducing cost and board space. Additionally, a faster switching frequency also

results in smaller ripple voltages and a faster loop response time to maintain regulation during transient loads. It is also desirable that a buck regulator that efficiently supports a high load-current, also efficiently drive light-load-currents. In many applications such as robotics and cellular phones, it is desirable that batteries last over long periods of stand-by or idle, wherein the output load is some nominal value relative to its maximum output capabilities.

By way of example, in a robot application it may be advantageous to use one high voltage battery system to power motors, analog, and high power digital systems. A higher battery voltage could be desirable because many motors operate more efficiently at higher voltages. The use of a buck converter to power the high power digital system is generally much more efficient than using a low drop out linear (LDO) regulator, especially when  $V_I$  is much higher than  $V_O$ . For example, if a robot with battery voltage  $V_I = 10V$  was required to be idle over night with  $f_s = 1MHz$ ,  $I = 100mA$ , and  $V_O = 1.8V$ , then using a standard buck gate drive as shown in Figure 3-1 could result in wasting over 200 times more power than if a low power buck converter was used at the same light-load, thereby substantially reducing battery life. As a reference, a linear regulator would be about 4-5 times less efficient at light and normal loads.

In this context, the present Thesis seeks to significantly increase the light-load efficiency of high power synchronous buck regulators at high switching frequencies, have high input voltages, and/or operate at light-loads.

### **Survey of Known Light-Load Efficiency Boosting Strategies**

A few known strategies exist to attain higher light-load efficiency; however, they rely on methods that are sometimes not impossible to implement, or do not achieve satisfactory electrical or cost performance. Known methods seek to adapt gate

capacitance, lower the gate drive voltage, or skip switching cycles as a way to increase efficiency of large FETs at light-load. The problem is that at light-loads, much more power is lost in turning on and off a large FET switch, than that lost to the resistance of the switch itself. At light-load, the  $f_s$  term of Equation (1) dominates, so prior-art seeks to minimize it (Tateishi 1999). As stated by Tateishi, it relates to a DC to DC converter which maintains high efficiency over broad current ranges in a current mode switching regulator circuit. The switching frequency is adjusted in accordance with the load without changing operational states, thus making it unnecessary to define plural states of operation. The timing of turning on the switches varies. For fixed frequency switching applications, switching pulses from a fixed frequency oscillator as a first set signal are skipped when a second set signal is not ready. Whereas, for a variable frequency, switching scheme which is implemented by driving the switching with a one-shot having a constant OFF time, the switching pulse is created after both set signals become active.

Such methods employ a burst mode that reduces  $f_s$  by passing more energy each time, and randomly turns on when needed. This is useful only in cases that can tolerate high ripple, and broad-spectrum noise. This is not acceptable in many high impedance analog and RF application.

A method of adapting gate capacitance, commonly referred to as gate splitting (Wilcox et al. 1998), dynamically selects a smaller switching FET under light-load conditions. Wilcox states that it provides switching regulator circuits in which the output circuit is adaptable to maintain high efficiency over various load current levels. The regulator circuits generate one or more control signals in response to the load current and selectively route a switch driver-control signal to one or more switches in the output

circuit. The switches differ in their size, such that the most efficient switch can be used at a particular load current level. At low load current levels, the driver control signal is routed to output circuitry with smaller switch devices, which incur smaller driver current losses for a given frequency of operation, thereby increasing the regulator efficiency. At high load current levels, the driver control signal is routed to large switch devices, which incur greater driver current losses for a given frequency of operation, but which have a lower impedance. The regulator thus maintains high efficiency over a wide range of load currents while operating at a constant frequency.

This approach reduces  $C_g$  with a smaller FET switch during light-load. This is a good strategy if the output FETs are integrated into the IC; however, if they are external it is very costly in parts, PCB area, and IC pin count, which are all unacceptable in most compact and cost sensitive portable applications. Furthermore, reducing  $C_g$  does not scale down to very small FETs because the resistance of the FET increase as the size of the FET decreases, thus significantly increasing the conduction, or DC, losses of the FET. For this reason, gate splitting begins to show benefit at higher switching frequencies than a low gate drive voltage,  $V_{gs}$ , approach. As shown in Equation (1) this is true because only a linear improvement to efficiency is achieved by the gate splitting approach, whereas decreasing the  $V_{gs}$  gate drive voltage has a square benefit.

The third degree of freedom is reducing  $V_{gs}$ . Synchronous buck switching regulator systems commercially available do not practice a low  $V_{gs}$  approach. However, a step-up, or boost, switching regulator application was found that generally implements the low  $V_{gs}$  concept (Muto 1995). Muto's approach, and others like it, simply lower the voltage supply that powers the gate drive circuitry shown in Figure 3-1. Muto uses a

linear regulator as the  $V_{gs}$  gate drive, voltage source for the output NMOS FET.

However, using a linear regulator to set  $V_{gs}$  is not possible at high  $f_s$  as the control loop of a linear regulator cannot act fast enough to provide the large, high frequency, nano-second current spike required to drive relatively large power MOSFETs. Moreover, the output voltage value of the linear regulator is predetermined, and cannot adapt to the various turn-on threshold voltages of arbitrarily selected output FETs. Additionally, Moto does not disclose or suggest a method or apparatus for limiting the P-side FET to  $V_I - V_{gs}$ , which is needed for a synchronous switcher topology.

Muto's approach may be practical in limited applications; however, it does recognize that there is a significant efficiency improvement benefit to reducing  $V_{gs}$  at light-loads. In view of Equation (1), given a squared loss penalty, there is clearly a much greater efficiency benefit in reducing  $V_{gs}$  over the other variables in the equation. Moreover, unlike only reducing  $C_g$ , which proportionately increases  $R_{dsON}$ , reducing  $V_{gs}$  significantly increases efficiency even at low frequencies.

An obvious way to reduce the gate drive voltage  $V_{gs}$ , while avoiding the impracticalities of using a linear regulator to power the gate-drive, would seem to be by way of detecting when the output FET turns on at the switch-node  $V_a$  and feedback this signal to turn off the gate drive circuit thereby avoiding FET overdrive. However, because at high switching frequencies the output FET must turn on and off faster than 10 ns it is not currently practical to efficiently construct a feedback mechanism that can respond within the required 4-10 ns to set the gate voltage correctly. There are two main problems. Firstly, a comparator must sample a relatively high capacitance node to detect when the FET is turning on, thereafter signal the gate drive to turn off, and wait through

propagation delay until the off signal reaches the gate driver output and begins to turn off the output FET. The propagation time of this feedback loop is simply too long and varies too much to set  $V_{gs}$  to a precise level that assures the FET is fully turned on, and at the same time is not being overdriven. Secondly, beyond the propagation time limitations of the feedback loop, the high current consumption, cost, and complexity associated with a very high-speed comparator is unacceptable for many applications.

A survey of the top vendors of catalog buck switching regulators ICs found no products on the market that implement any light-load efficiency strategies for large external FETs that must operate in a synchronous mode. In particular, no buck regulator products on the market limit  $V_{gs}$ , or recycle parasitic energy as an efficiency boosting strategy. Thus, their efficiencies are often below 20% at low milliamp loads when forced to operate in the low noise synchronous mode.

In view of the foregoing, a need exists for a practical technique to improve the power efficiency of relatively high power synchronous buck, switching regulator operating at light-loads. This method should automatically adapt to the selected output FETs, while not increasing cost or complexity. It would also be desirable if solution to the light-load efficiency problem also provided a means of detecting the light-load condition.

## CHAPTER 4 RECYCLED GATE DRIVE ENGERGY

### **Approach**

It is recognized that power MOSFETs have a substantial amount of parasitic capacitance between the gate and source ( $C_{gs}$ ) and between the drain and source ( $C_{ds}$ ). Typical values for  $C_{gs}$  can range between 400-1000 pF and  $C_{gd}$  between 80-200 pF. Moreover, when placed in a practical circuit, there are other inductive and capacitive parasitic elements that further increase the overall parasitic content of nodes such as the common switch-node ( $V_a$  in Figure 3-1) between push-pull, or totem-pole, configured MOSFETs. In general, known structures inefficiently switch totem-pole configured MOSFETs by failing to recognize that a substantial amount of the energy necessary to turn a MOSFET on could be provided by otherwise wasted energy stored in inductive and capacitive elements on the common switch-node of the totem-pole connected MOSFETs. Moreover, in the field of switching regulators, no known prior-art exist that uses energy from the switch-node to turn on the output power MOSFETs.

The present approach significantly improves the switching efficiency of totem-pole configured MOSFETs by using the switch-node as a source of “free” energy to turn on the MOSFETs. A significant amount of energy that past methods waste can be recirculated to drive the output MOSFETs. This energy is enough to initially turn-on the large output MOSFETs, and then only a small amount of energy is needed to bring  $V_{gs}$  to its final voltage. This technique represents a substantial departure from the common

wisdom in buck regulator design, while achieving light-load efficiency performance very difficult to achieve otherwise given current technology.

To implement the above concepts, it is important that there be maximum flexibility available to the designer to adjust all parameters necessary to meet certain specifications of a given application. The design must also be very robust, and have typical failure modes that still permit useful, but possibly less efficient, operation. The buck switching regulation topology will be based the standard gate drive design shown in Figure 3-1 with a few modifications. The novel contribution is in the way the gate drive circuits turns on the main output MOSFET's. Current gate-drive circuit designs have a very large MOSFET that pulls energy from the power supply and dumps it to the gate of output MOSFET to turn on. Because the amount of energy used to turn on the output MOSFET is largely independent of loading, there is a significant power efficiency penalty at light-loads.

There are additional benefits resulting from the present design. In one aspect, the recirculated energy transfer from the inductor to the gate drive occurs so fast that the output MOSFET is turned on almost instantly (i.e., within a few nanoseconds), which is normally too costly for known methods in terms of die area, current spikes, and power consumption. Another benefit is that once the worst case conditions are designed for the present system automatically adjusts to a wide range of off-the-shelf output MOSFETs. Additionally, as will be shown below, a self-clamping mechanism inherent in the present architecture eliminates the need for an external Schotkey diode (D1 in Figure 3-1) that known methods require. The design also has the full design flexibility required to achieve maximum robustness, while still providing significant efficiency benefit.

Moreover, the present method is transparent to the user and backwards compatible with systems using prior buck designs.

### **Implementation of Parasitic Energy Recycling**

The design illustrated in Figure 4-1 switches transistors MP0 and MN0 alternately on and off in response to the input control signals P\_DRV and N\_DRV, respectively. They are switched in such a way that they operate functionally as in prior-art, except that gate drive energy is stored and received from the switch-node SWn, instead of the ground and power supply respectively. The design shown demonstrates one practical implementation of the present concept that provides for control-signal conditioning and a mechanism to recycle a portion of MP0 and MN0 gate drive charge. Transistors Q0 and Q1 are the controlled path to store and supply gate drive energy respectively. For clarity, bipolar transistors are shown as conceptual devices. Actual implementations usually use MOSFETs. Transistors MP2 and MP5 are added for robustness, thereby ensuring that MP0 and MN0 turn on. They are sized such that they are large enough to provide the threshold turn-on gate charge needed, which the SWn through Q0 and Q1 cannot alone provide. The gate drive transistor Q0 that turns on the main PMOS device, and the gate drive transistor Q1 that turns on the main NMOS device, however, each have their emitter and collector, respectively, referenced to the switch-node (SWn) instead of ground or  $V_{dd}$ , respectively, as in prior-art designs.

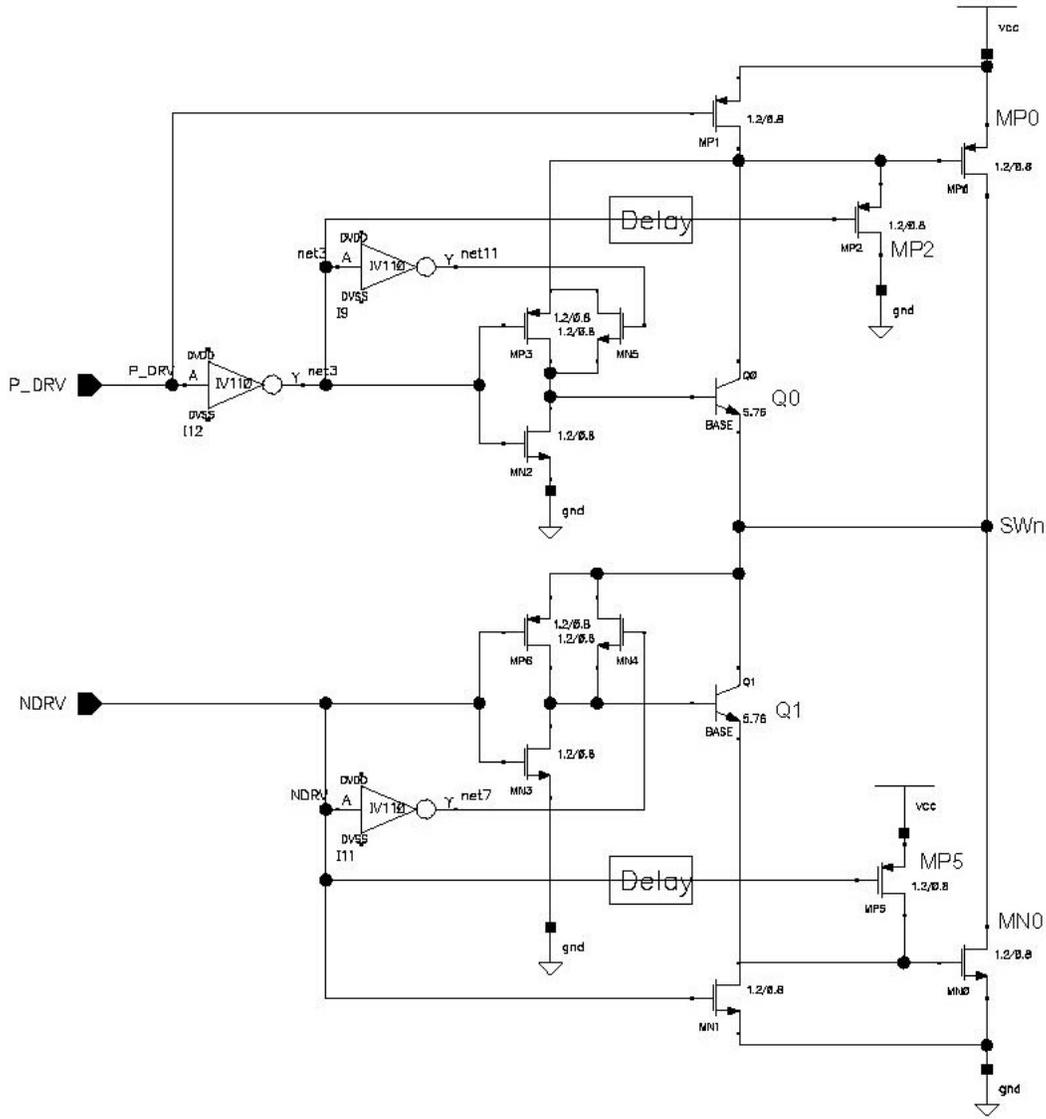


Figure 4-1 A physical implementation of the energy recycling system.

The conceptual structure of the present approach is shown in Figure 4-2. Q1 and Q2 are effectively directed switches that pass current only in the direction of the arrow as illustrated by using a NPN transistor conceptual device. The blocks labeled “D” are delay lines that allow the Q1 and Q2 to transfer recycled energy before adding any energy from the power supply, if needed.

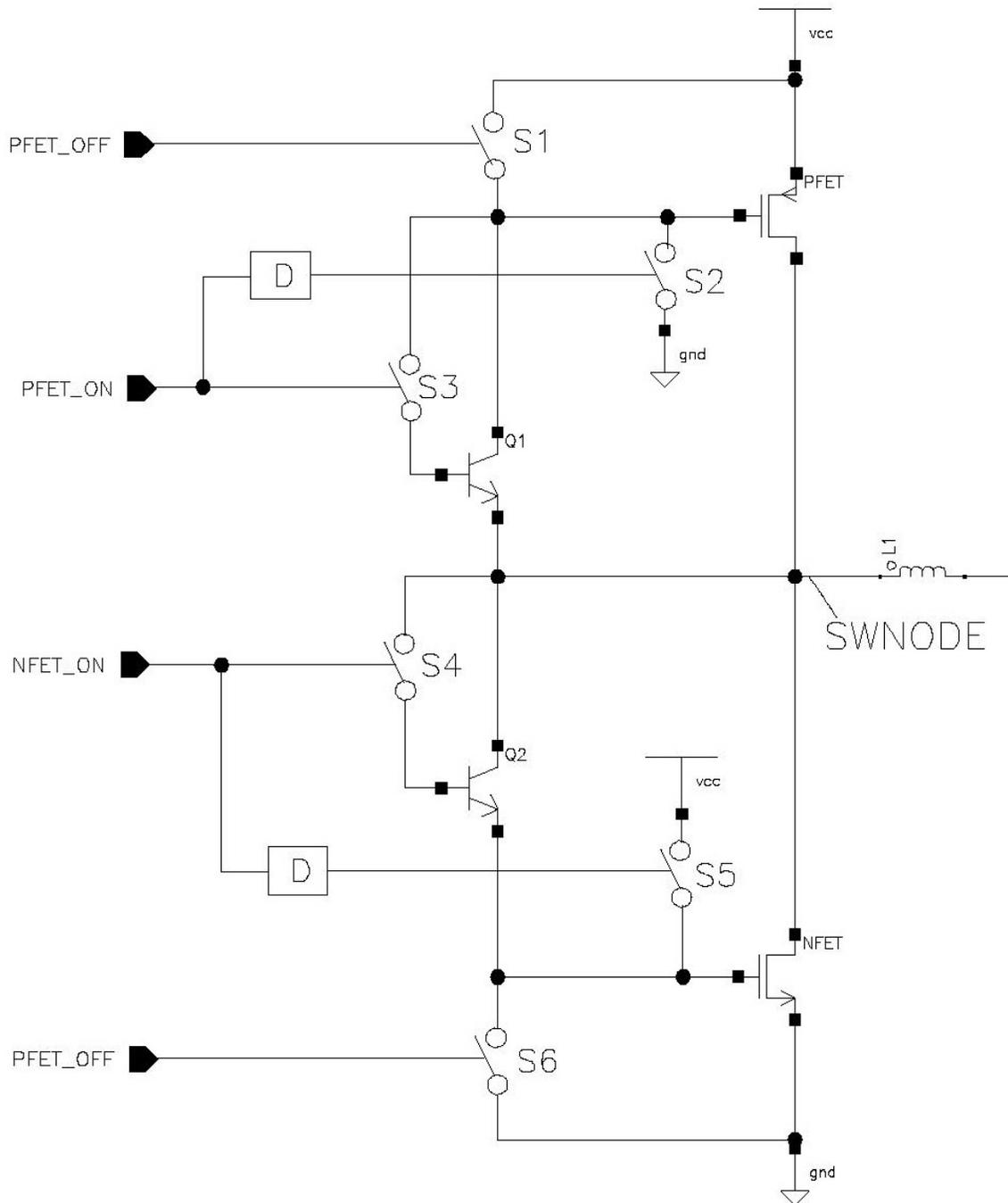
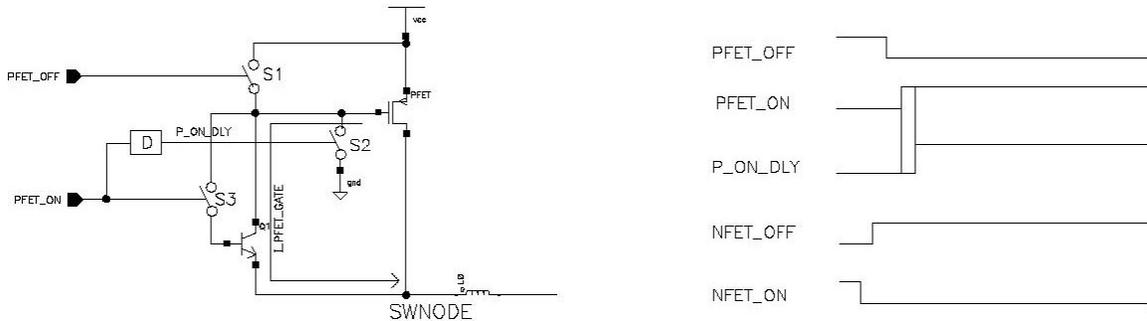


Figure 4-2 A conceptual view of the energy recycling system.

Figure 4-3 depicts the flow of gate charge out of the output PFET and into the energy storage elements of the switch-node when the output PFET is being turned on and the output NFET off. To the right of the schematic are the related controls and timing

signals. After this phase is complete, the output switch-node voltage is near the power supply voltage. Once the PFET is on, and the NMOS off, the switching node is guaranteed to have switched to a supply potential opposite that established just before its state change, which in this example is equal to the supply potential.

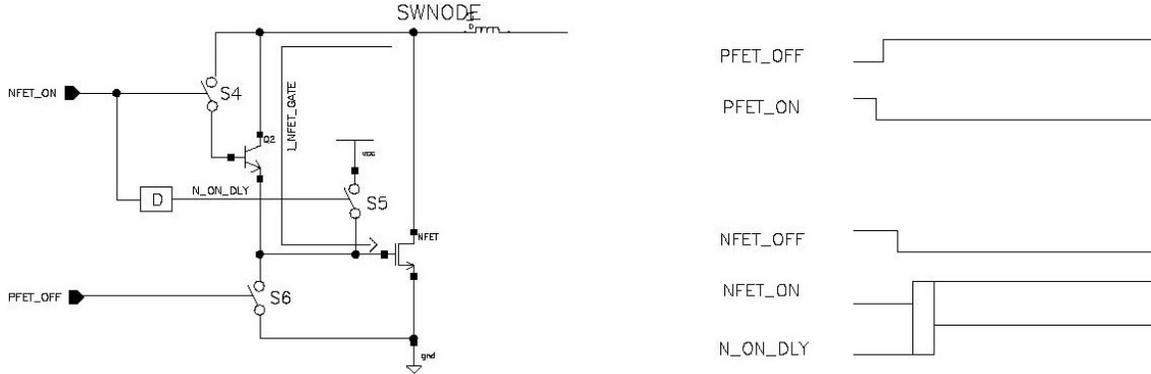


Timing diagram for turning NFET off & PFET on

Figure 4-3 Control signals and active components for the output high phase.

In Figure 4-4, the energy recycling procedure of this design is completed by transferring charge previously stored into the switch-node to the gate of the output NFET. To the right of the schematic are the related controls and timing signals. Once the NMOS is on, and the PFET off, the switching node is guaranteed to have switched to a supply potential opposite that established just before its state change, which in this example is near the ground potential.

In each case, the output FETs are turned off as in prior-art and turned on as prescribed by this presented method. A key enabling aspect the design is that the switch-node is always guaranteed to be in an opposite charge state than that of the FET to be turned on. This ensures that the switch-node will always be able to provide, to some degree, FET turn on energy that would have otherwise been recombined with the power supply.



Timing diagram for turning PFET off & NFET on

Figure 4-4 Control signals and active components for the output low phase.

In a particular embodiment of this technique, an inductor is connected to the switch-node, as would be done in a DC-DC switching regulator. Typically, the switch-node will have significant capacitive parasitics from the output FETs and possibly a Schottky clamping diode. To some limit, the larger the effective inductance and capacitance of the switch-node, the more energy that can be recycled as prescribed by the presented method.

Importantly, most of the requisite energy is provided by the output parasitic capacitance and inductance at the switch-node. Known structures and techniques actually waste this energy back to the supply. In contradistinction, using the inventive techniques described above, the gate drive is seen to receive more “free” energy from the switch-node as the switch-node parasitics value increases, given that there is more energy stored for recycling. Given current technology, to achieve the same  $R_{dsON}$  as an NFET, the PFET usually has a higher gate capacitance  $C_{gs}$ . Hence, there is enough gate energy to turn on the NFET if it can be adequately transferred from the PFET. It is a good practice

to keep the  $C_{gs}$  of each FET roughly equivalent to ensure that adequate energy to turn each FET on can be sourced or synched from the parasitics at the switch-node.

### **Conclusion**

In summary, the present high efficiency MOSFET switching technique recirculates gate drive charge, thereby providing a substantial portion of the gate drive energy necessary to drive the output FET devices, while providing a significant power efficiency boost. Known structures waste gate drive charge by failing to recognize that most of the energy necessary to turn a FET on could be provided by the otherwise wasted energy of the complement FET being turned off. The on-time gate driver FET recirculates “for free” most of the needed gate drive energy from parasitic energy storage components at the switch-node. No known methods implement this novel approach. Instead, prior approaches waste the parasitic energy stored at the switch-node and use the power supply to drive the gates.

In particular, when the present approach is applied buck synchronous regulators, a significant efficiency increase in both light and normal load conditions is observed- as will be shown in the results section of this Thesis. The results show that the parasitic energy at the switch-node is enough to turn on the output power FETs. Hence, it can be deduced that a significant amount of the efficiency boost occurs because most of the energy required to turn a FET occurs at turn-on due to the Miller effect. Moreover, because the transfer of recirculated energy from the inductor to the gate drive occurs so fast, the output FET is almost instantly turned on. This fast switching speed is normally prohibitive in a prior-art design and provides added efficiency benefits by minimizing the time that the output FET is in a partially-on state. It is well known that the longer it takes

to turn on a FET, the more power is lost to transient variations of voltages and currents within the FET.

In the context of practical implementation, the system designer has full flexibility to take advantage of the light-load efficiency benefits presented, while ensuring robust operation by way of adding a small “helper” gate drive FET. The helper FETs provide the small amount of energy required to ensure the output FET is completely turned on, independent of the supply voltage and load-current. Once designed for the worst-case conditions, the present system automatically adjusts to a wide range of output FET sizes and turn-on threshold voltages.

The present method also provides benefits at normal load operation by assisting the on-time driver FET to quickly turn on the output FET thereby permitting a smaller on-time driver FET than would otherwise be possible. Thus, there is no significant additional cost or complexity in implementing the present design in the context of prior-art buck regulator systems. This is true because the present design uses same total FET area of a prior-art design, and simply redistributed these assets with a slightly different hookup. Moreover, the gate drive controller is essentially the same as prior-art and the gate drive circuit is simply split into separate functional blocks and timed differently.

## CHAPTER 5 SYNCHRONOUS BUCK REGULATOR LIGHT-LOAD DETECTION

### **Approach**

The technique herein presented seeks to detect when a synchronous buck regulator enters a light-load state that is characterized by output load-currents that are below some predetermined threshold. In particular, the present method senses the switch-node (SWnode) as a light-loading indicator. Known methods detect light-load by adding a sense resistor in the conduction path, or by sensing a voltage rise in the regulator's output. The result of these standard methods is to add costly components to detect light-loads. Known structures inefficiently detect light-loads by failing to recognize that assets already employed in synchronous switching regulators can also serve to detect a light-loading operating point. In particular, when the buck regulator enters discontinuous mode there is a positive-going signal that detected at the switch-node. Because the discontinuous mode occurs when the load-current drops below a certain level set by the buck inductor value, the discontinuous mode can be effectively used as a proxy for detecting a light-load condition.

### **Theory of Operation**

The goal of the design is to provide an efficient and practical method to determine when a switching DC-DC regulator is under a light-loading condition. The point where the switching losses dominate over DC conduction losses characterize the light-load condition. However, for the purposes of this invention, "light-load" is defined as a range of operating points near, and not necessarily equal to, the aforesaid definition.

Figure 5-1 demonstrates one practical implementation of the present approach that for detecting light-loading conditions. The RSTB signal sets initial condition ( $Low\_I="0"$ ) when RESETB starts out low. Upon detecting a positive going zero crossing voltage, a short active-high pulse will be generated at node ZERO\_CROS. If there is no zero crossing event for two consecutive CLK\_IN cycle LOW\_I will be reset to Low. This mechanism filters out typical short duration system noise. The rising edge delay block and the AND gate(I1) are introduced so that the “kick-back” glitch when N\_DRV changes from low to high is suppressed when N\_DRV is set hi. In this way, light-load conditions are sensed by positive going switch-node voltages during the discontinuous operating phase of the switcher. Energy is supplied to the switching node via an inductor with current waveforms as illustrated in Figure 5-2. The output load-current is simply the average inductor current, marked by the  $I_0$  line. The constant amplitude triangular current waveform shifts up and down directly with the output load-current,  $I_0$ . When the switch-node voltage goes positive, the inductor is devoid of current and is charging in the reverse direction. This crossover, or discontinuous operating, point is load dependent and occurs when the average output current  $I_0$  minus half the switching current  $I_{SW}$  goes negative; or *light\_load* is when  $I_0 - 0.5 * I_{SW}$  is less than or equal to zero. Figure 5-3 shows the onset of the discontinuous operating mode. The switching current  $I_{SW}$  is a function of the , duty cycle, which depends on supply voltage, switching frequency, and passive components. Those experienced in the art of switching regulator design can select the inductor value that meets specifications under worst-case operating conditions, whereby a desired range of *light\_load* trigger points can be reliably set.

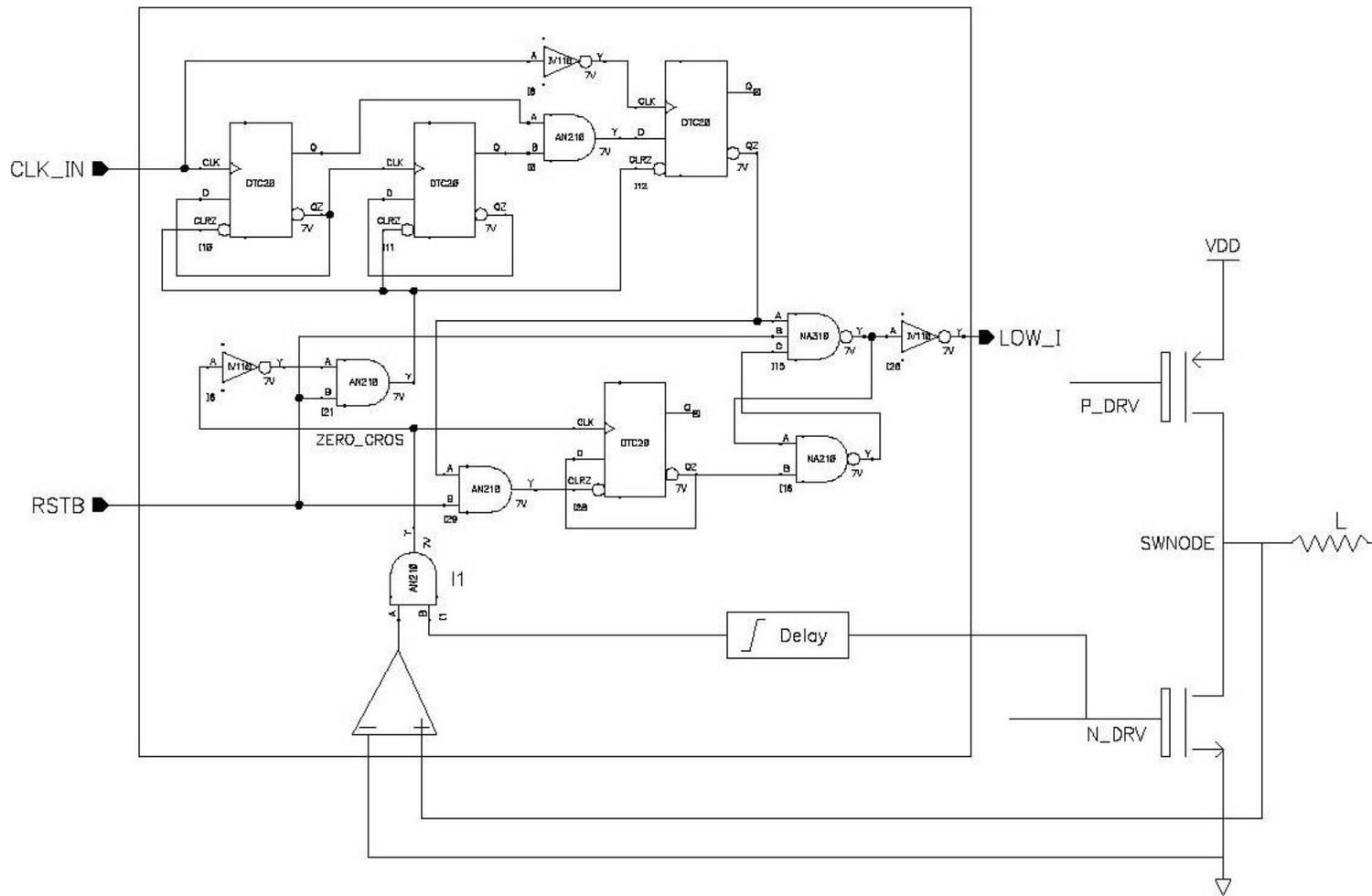


Figure 5-1 A circuit implementation of the light-load detection system.

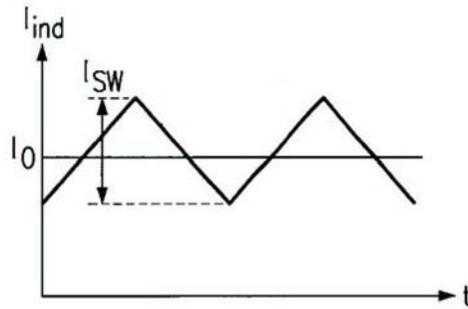


Figure 5-2 Inductor current ( $I_{ind}$ ) at normal load over two full switching cycles.

For many practical systems it is very useful to know, even if only approximately, when the switching regulator is not under significant loading. To detect a light-loading condition, known structures and techniques add inefficient and expensive current sensing components such as resistors, comparitors, and voltage references. Those skilled in the art of synchronous DC-DC switching regulators will know that these assets are already available and necessary to turn off the synchronous FET when in the discontinuous switching mode. Thus, current systems add significant cost and complexity to achieve high precision light-load detection, when inherent system components could be used to provide lower precision, but sufficient, light-loading information at no substantial cost or complexity.

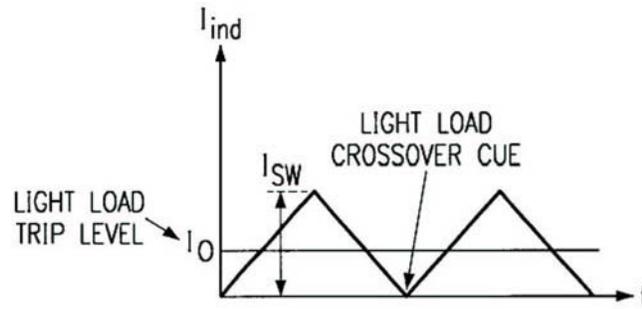


Figure 5-3 Inductor current ( $I_{ind}$ ) over two full switching cycles at light-load onset.

### Conclusion

In summary, the present synchronous switching DC-DC switching regulator, light-load detection technique provides a mechanism to determine a general light-loading condition without additional components. Known structures incur significant costs and energy loss by failing to recognize that for most applications, light-load detection could be achieved with existing assets as prescribed by the presented technique, instead of adding a higher precision, and high cost detection systems.

Beyond the cost benefit of the presented approach, there is the additional benefit of increased power efficiency, especially at high current loads, by eliminating the series current sensing resistor (typically 50-100 mOhms) implemented by most known designs. When compared to the typical power FET on resistance of 20-100 mOhms, it is seen that the present technique can provide a significant benefit to efficiency by reducing the conduction path parasitic resistance by one half or more.

## CHAPTER 6 SYNCHRONOUS BUCK LOW VOLTAGE GATE DRIVE

This chapter sets forth several novel methods to achieve robust low voltage gate drives for MOSFETs arranged in a binary, push-pull configuration.

### **Low Voltage Gate Drive Architectures**

#### **Basic Approach**

To increase switching power efficiency of push-pull configured MOSFETs, the methods presented in the sections that follow all limit the gate drive voltage swing to a level that is significantly less than the input supply voltage. Figure 6-1 illustrates the basic conceptual output stage hookup. In common with the gate-voltage setting mechanisms that follow is the use of the switch-node (SWnode) as the control reference for the  $V_{gs}$  gate drive limiting process. Furthermore, the appropriate on-time gate drive FET behaves as the controlled switch. Throughout, these on-time gate drive FETs will be referred to as PonSW for the gate drive FET that turns on the main PMOS (PMOSmain), and NonSW, likewise, for that of the main NMOS (NMOSmain). It will be appreciated that not only does the switch-node exactly time the  $V_{gs}$  setting process, but, as discussed in the energy-recycling chapter above, the switch-node also supplies most of the energy needed to turn on the main FETs. An important departure from prior-art MOSFET switching designs is that PonSW and NonSW have their sources referenced to the switch-node, instead of the respective positive ( $V_{dd}$ ) or negative (**gnd**) power supply connections.

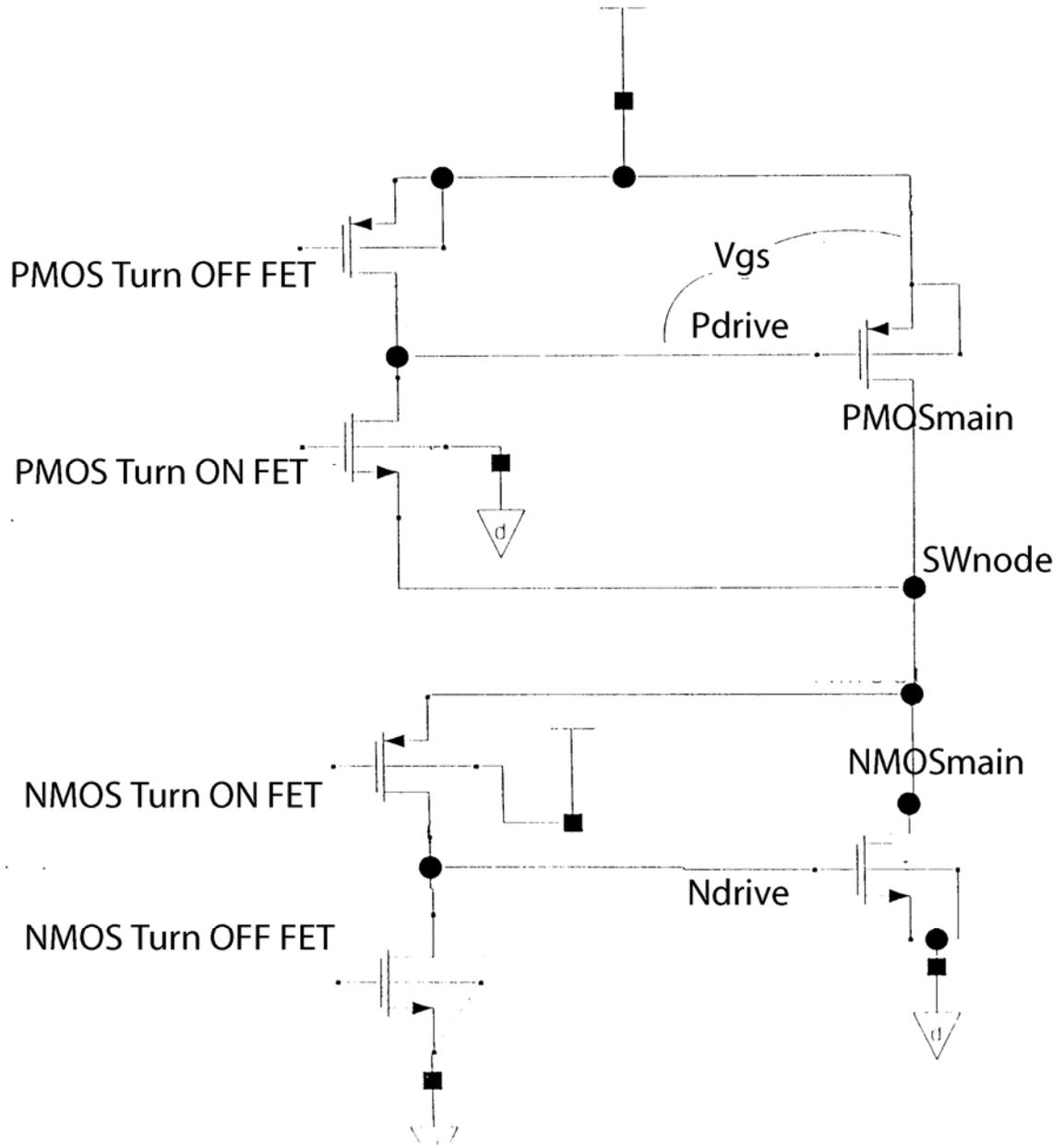


Figure 6-1 Top level low  $V_{gs}$  output stage design.

As in prior-art methods, the voltage setting process according to the present method begins by appropriately applying  $V_{dd}$  or gnd to the turn-on FET that corresponds to the main output FET to be turned on.

## Output MOSFET Turn On Mechanism

The first step of this  $V_{gs}$  setting procedure is to turn-on the appropriate output MOSFET. The following example is given with reference to the implementation details shown in Figure 6-1. If it is assumed that the current state of SWnode is at the  $V_{dd}$  potential (i.e., PMOSmain on and NMOSmain off), then the next step is to toggle the state of all the gate drive signal, whereby NonSW and PonSW would be activated and the Noff and the PonSW are deactivated. This operation results in SWnode being connected to ground through NMOSmain. To switch SWnode back to the  $V_{dd}$  potential the opposite set of gate drive FETs would be activated. While in synchronous mode, each time a turn-on FET is activated the SWnode is guaranteed to be at the opposite voltage potential than the gate of the turn-on FET. To continue the prior example of switching the grounded SWnode back to  $V_{dd}$ , it is observed that the PonSW will have  $V_{dd}$  applied to its gate and ground at its source resulting in a  $V_{gs} = V_{dd}$ . Because PonSW is of the NMOS type it will be fully turned on and current will rush from Pdrive to SWnode thereby pulling down Pdrive and pulling up SWnode until  $V_{gs}$  drops below the threshold voltage required to keep the NMOS turned on. As illustrated in Figure 6-2 with  $V_T = 1V$  and  $V_{dd} = 2.8V$ , the point where  $V_{SWnode} = V_g - V_T$  is referred to as the crossover point because above this point  $V_{gs}$  is less than  $V_T$  and the NMOS turns off thereby setting  $V_{Pdrive} = V_g - V_T$ . It should be noted that  $V_{Pdrive}$  reaches its value at the crossover point in a very smooth manner and with little overshoot. This occurs because the NMOS gate drive transistor turns off smoothly as its  $V_{gs}$  approaches  $V_T$ . It should be noted that the present methods achieve more robust and efficient operation when the drain current being conducted by the MOSFET ( $I_D$ ) at turn on is relatively low. This is true because the  $V_{gs}$  required to achieve a certain on-resistance value ( $R_{dsON}$ ) increases with  $I_D$ . For many power

MOSFETs this  $V_{gs}$  is flat up to about 0.5-1A and then logarithmically increases with  $I_D$ . It should also be appreciated that the same analysis presented above applies to the  $V_{gs}$  setting mechanism for NMOSmain except that the respective signal polarities are reverse.

### **Discontinuous Mode Issues and Self-clamping**

The above set/reset process alternates with each ON/OFF pulse width modulation (PWM) cycle in each switching period. However, before turning on an output FET it is important that SWnode be in the same state resulting from the last transition. This is generally guaranteed in synchronous modes of operation and for the N-drive. A problem, however, arises for the P-drive from the discontinuous operating mode because SWnode can be left floating thereby resulting in a low energy, dampened sinusoidal ringing that may not give sufficient voltage difference to pull down Pdrive. The worst case is when  $V_{SWnode}$  is past the crossover point, or  $V_{SWnode} > V_{set} - V_T$ , where  $V_{set}$  is the value of  $V_g$  that is set equal to the desired terminal  $V_{Pdrive}$ . The solution for this ringing problem is to force SWnode to **gnd** just prior to turning on the PMOS. A unique “self-clamping” technique is implemented that uses the energy in the SWnode to turn on the main MOS thereby grounding SWnode. This clamping, or “snubbing,” mechanism works by turning on the gate driver of the opposite main MOSFET to that which is to be turned on. Referring again to Figure 6-2, a self-powered snubbing event is shown where the Ndrive, driven by the SWnode, is pulsed to ground the discontinuous mode ringing just prior to turning on the main PMOS. The self-snubber requires  $V_{SWnode} > V_T$  to turn on the main NMOS. If  $V_{SWnode} < V_T$ , a much smaller prior-art snubbing NMOS is sufficient to ground SWnode. As described for the synchronous case, once SWnode is clamped to either **gnd** or  $V_{dd}$ , as appropriate, the main FET gate can again be driven by the SWnode until the crossover point is reached. It should be appreciated that

by using the ringing energy, that is normally wasted, to snub itself, we avoid the significant energy cost of potentially turning on a large snubbing FET every cycle as occurs in many known approaches.

### **Post Turn-on Gate Drive Behavior**

After the crossover point is reached, the main FET has been turned on and the gate and drain of PonSW and NonSW effectively reverse whereby SWnode acts as a power source that force Ndrive and Pdrive to within a  $V_T$  of  $V_{dd}$  and **gnd** respectively. At the end of the post turn-on phase, each output MOS is guaranteed to be marginally ON. This is a key feature of the design. That is, the gate drive automatically adjusts itself to turn on the main FET, and bootstrap the main FET's  $V_{gs}$  to  $V_T$ . As will be shown below, the next step is to activate a  $V_{gs}$  setting phase that gently tugs the main FET's gate voltage to a desired set point.

It is useful to note that the smaller  $V_T$ , the more energy that is transferred from SWnode to the main MOS gate drives. Hence, PonSW and NonSW are preferably low  $V_T$  devices. The higher  $V_T$  the larger the switch-node connected gate drive FET needs to be to guarantee to transfer enough energy to turn on the main FET's with energy from SWnode.

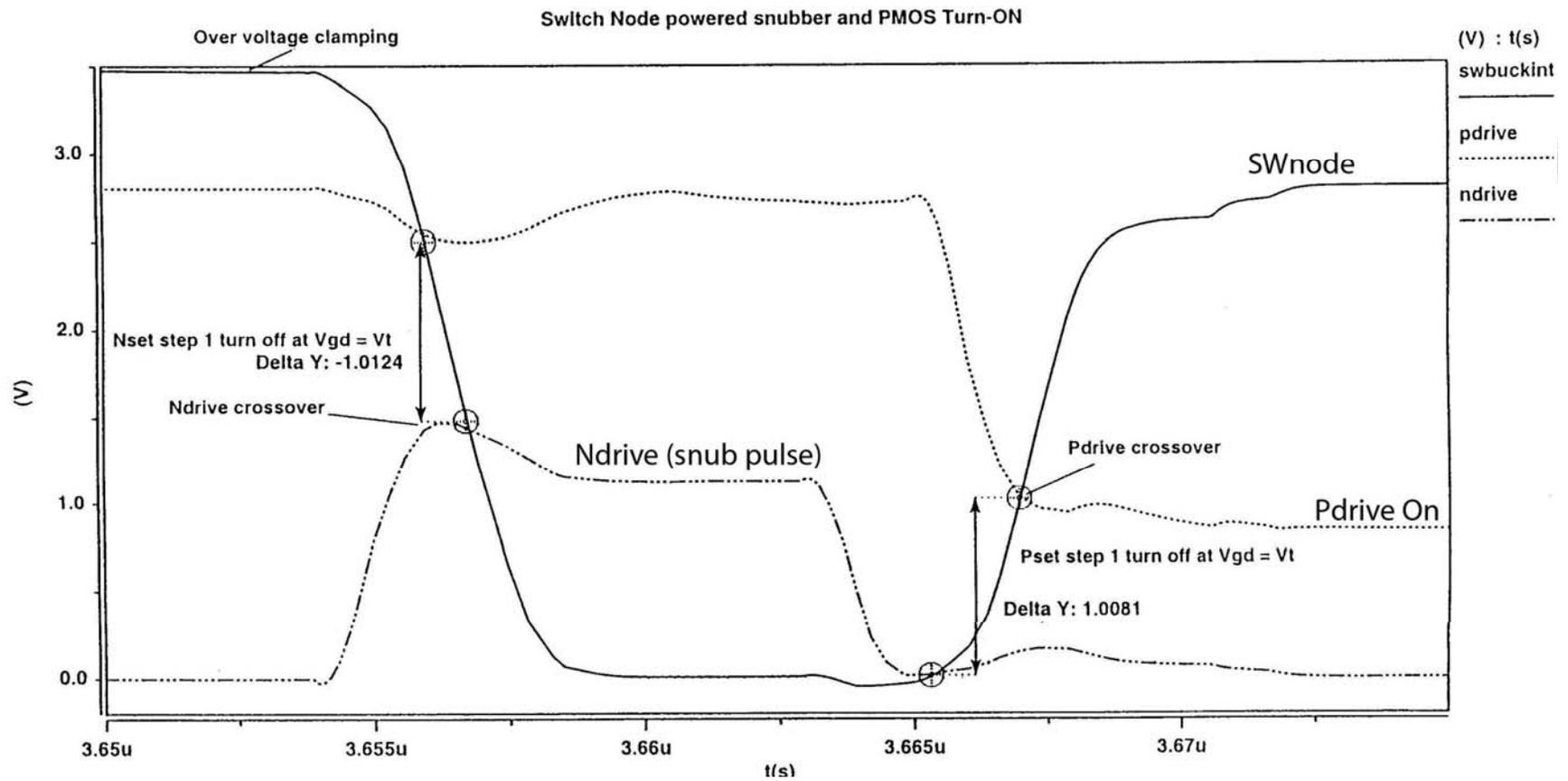


Figure 6-2 Gate drive signal for self-snubber and PMOSmain turn-on.

### **Gate Voltage Setting Phase – Output MOSFET Full Turn-on**

After the main output FET is turned on during the turn-on phase  $V_{gs} \approx V_T$ , the next step is to implement a gate voltage setting (Vset) procedure. The cue for this step is when SWnode is within  $V_T$  of its final state, indicating that the appropriate output MOS is fully on; i.e., the turn-on phase is complete. In the Vset procedure, the gate drive is turned off by putting it in a high-impedance output state, and a Vset block is activated. The Vset mechanism can take several forms depending on the needs of the application. Five novel Vset mechanisms are set forth in the sections that follow. The basic forms presented below are as follows:

1. Diode drop clamping.
2. Linear regulator.
3. FET clamping with reference voltage (Vref), where Vref is set by various combinations of resistor/diode and current source or as in item 2 above.
4. Switch-node FET clamping with reference voltage as in item 3, above.
5. FET forcing of Vset with reference voltage as in item 3, above.

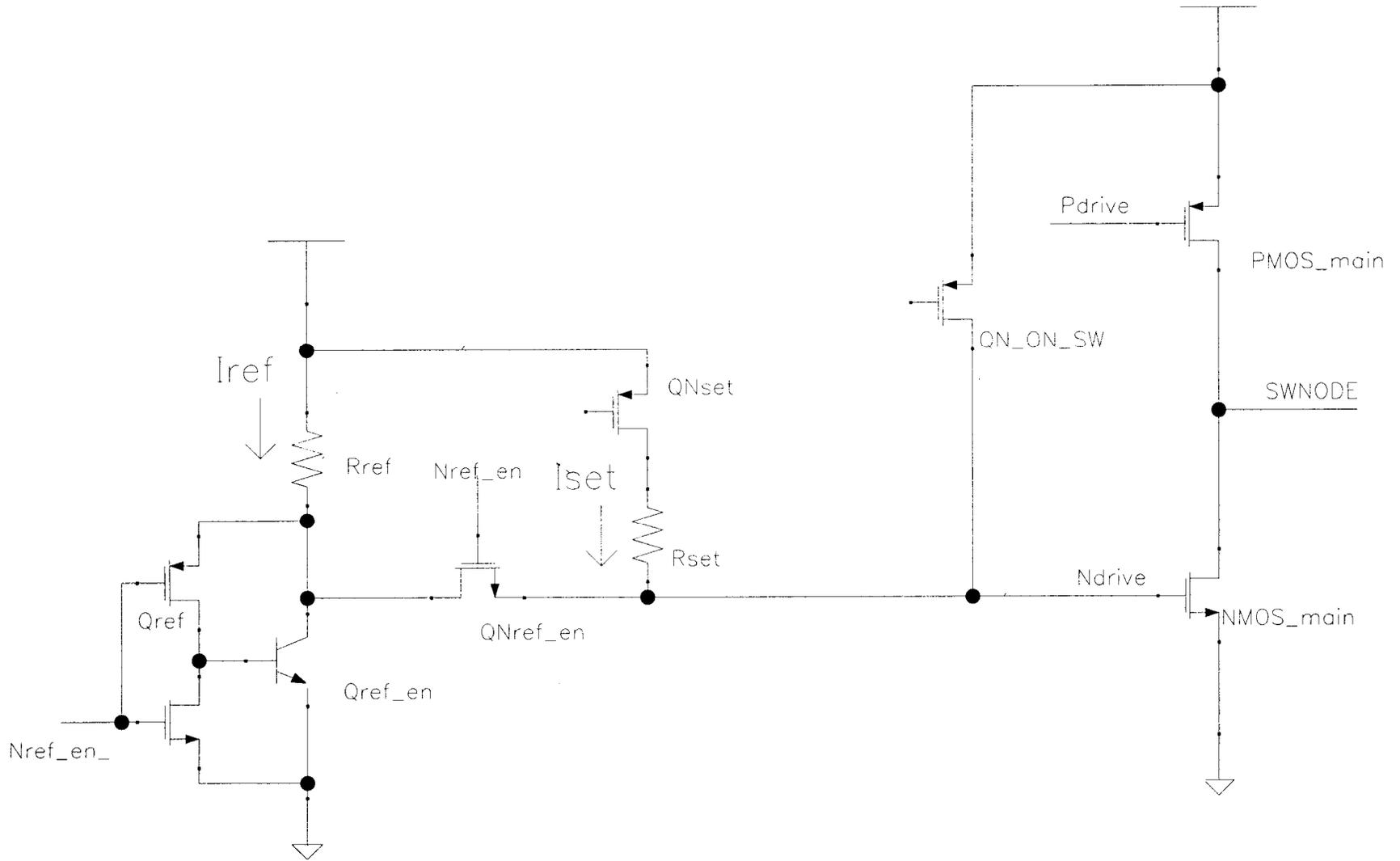


Figure 6-3 Diode drop gate voltage setting circuit.

### Gate voltage setting via diode drop clamping

Figure 6-3 illustrates a typical circuit implementation of a diode drop clamping system, exemplified for the Ndrive side, but similarly applicable to the Pdrive side. In this case, the  $V_{gs}$  setting process centers around using the  $V_{be}$  drop of a diode connected NPN transistor  $Q_{ref\_en}$  as a reasonably good band gap reference. The  $Q_{ref}$  FET activates the diode reference in response to the active low  $N_{ref\_en}$  signal thereby generating reference current  $I_{ref}$  through resistor  $R_{ref}$ . Simultaneously,  $Q_{N\_set}$  forces Ndrive, and thereby the NMOS\_main  $V_{gs}$ , to a voltage determined by the voltage division between the diode and a resistor  $R_{set}$ . For stability over temperature,  $Q_{ref}$  and  $Q_{Pset}$  FETs should be large enough that their  $R_{dsON}$  is much less than  $R_{set}$ . This requirement is due to the large variation (up to 200%) of a FET's  $R_{dsON}$  and hence,  $V_{set}$ , versus a discrete resistor's less than 10% variation over temperature. Given that  $V_{be}$  is exponentially dependent on current  $I_{set}$ , any process variations in  $I_{set}$  causes much less change in  $V_{be}$ . The reference turn-on switch,  $Q_{ref}$ , is placed in the base-collector path to reduce its size given  $I_b$  is much less than  $I_c$ .

The present method works by charging the gate capacitance ( $C_g$ ) of NMOS\_main with  $R_{set}$  until the diode turns on and clamps the node to  $V_{set}$ . The value of  $I_{set}$ , as determined by  $R_{set}$ , will drive the gate voltage setting speed and the diode voltage drop. These parameters also increase with  $V_{dd}$  as illustrated in Figure 6-4. In the Figure, the N-drive  $V_{gs}$  set voltage is seen to increase with  $V_{dd}$  over a supply range of 2.8-5.5V. The N-drive  $V_{gs}$  set point was targeted for 2V at 3.6V. For the operating range of 2.8-4.2V, there is only a +/- 12% change in the  $V_{gs}$  set point. A wide range of  $V_{gs}$  set points can be achieved by modifying  $R_{set}$ ,  $R_{ref}$ , and the diode's  $V_{be}$ . The present design shown in the

circuit of Figure 6-3 is particularly useful when accuracy is not significant, and simplicity is more important. Similarly, Figure 6-5 graphs the variation of the P-drive with  $V_{dd}$ . The curves are normalized to a 5.5V reference point for easier comparison. It is seen that the P-side experiences significantly more setting error at higher voltages due to a significantly greater  $V_{gs}$  differential voltage, than that for the N-side.

### **Gate voltage setting via linear regulator**

A linear regulator can be added to increase voltage-setting accuracy. A circuit that implements this approach is instantiated in Figure 6-6. In the Figure, a low drop out regulators (LDO) is used as a fixed voltage reference to achieve very accurate setting accuracy by fixing  $I_{set}$ , and  $V_{be}$  to a repeatable value independent of  $V_{dd}$ . The penalty, though, is increased cost and higher quiescent current consumption. Normally gate drive efficiency suffers greatly when supplied by a linear regulator. However, as the switch-node already turned on the output FET, and thereby supplied its Miller capacitance, only a very small current (in the low milliamps) is necessary to set the final  $V_{gs}$ . In contrast, if the LDO was used to turn on the output power FET, the impact to light-load efficiency would be far more significant, as is the case in prior-art. The typical variation of  $V_{set}$  with  $V_{dd}$ , while holding  $V_{ref}$  and diode parameters constant, is very low.

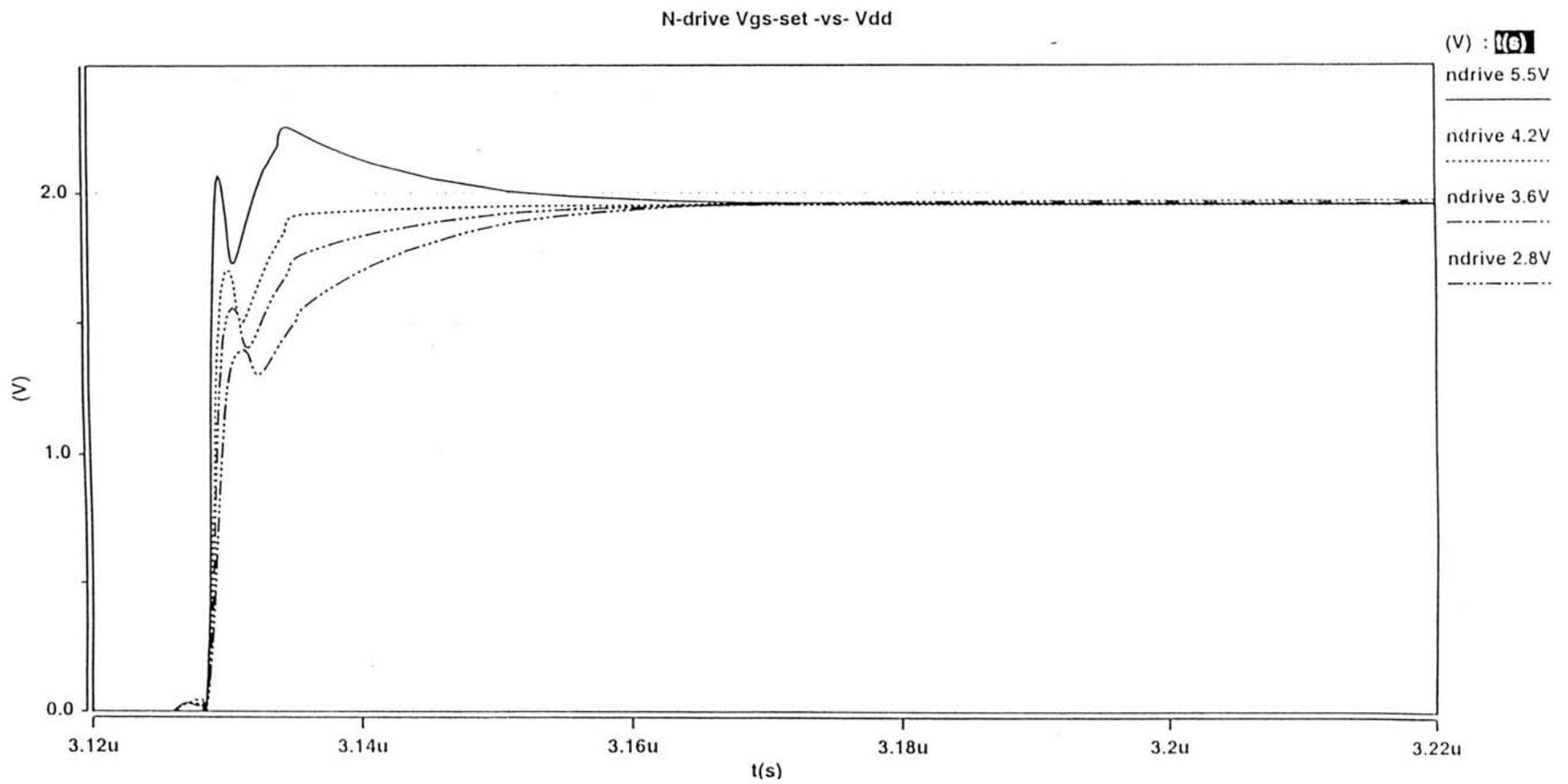


Figure 6-4 N-drive gate voltage setting family of curves for  $V_{dd}$  from 2.8-5.5V.

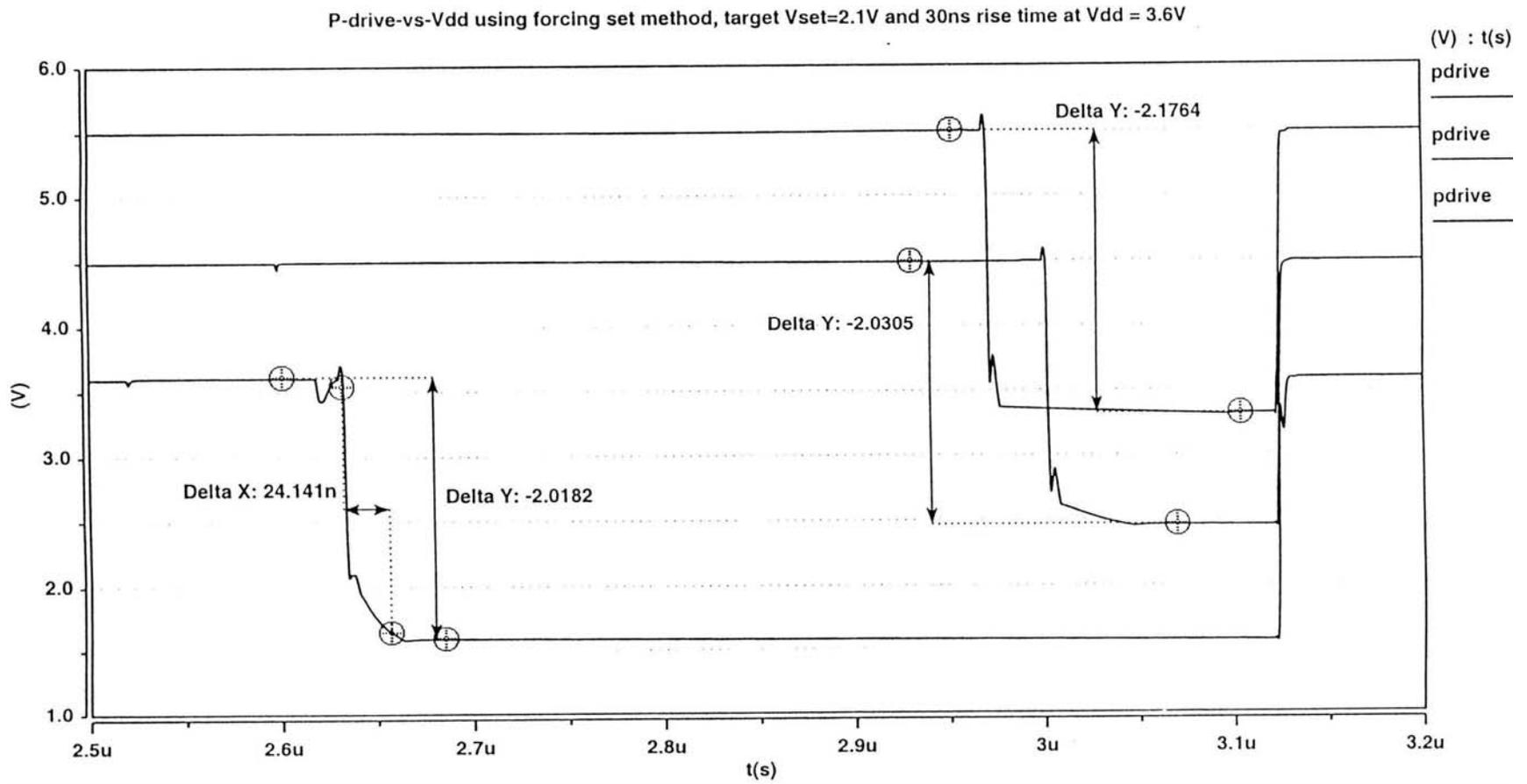


Figure 6-5 P-drive gate voltage setting family of curves for  $V_{dd}$  from 2.8-5.5V.

Diode clamping Vgs setting method with linear regulator reference

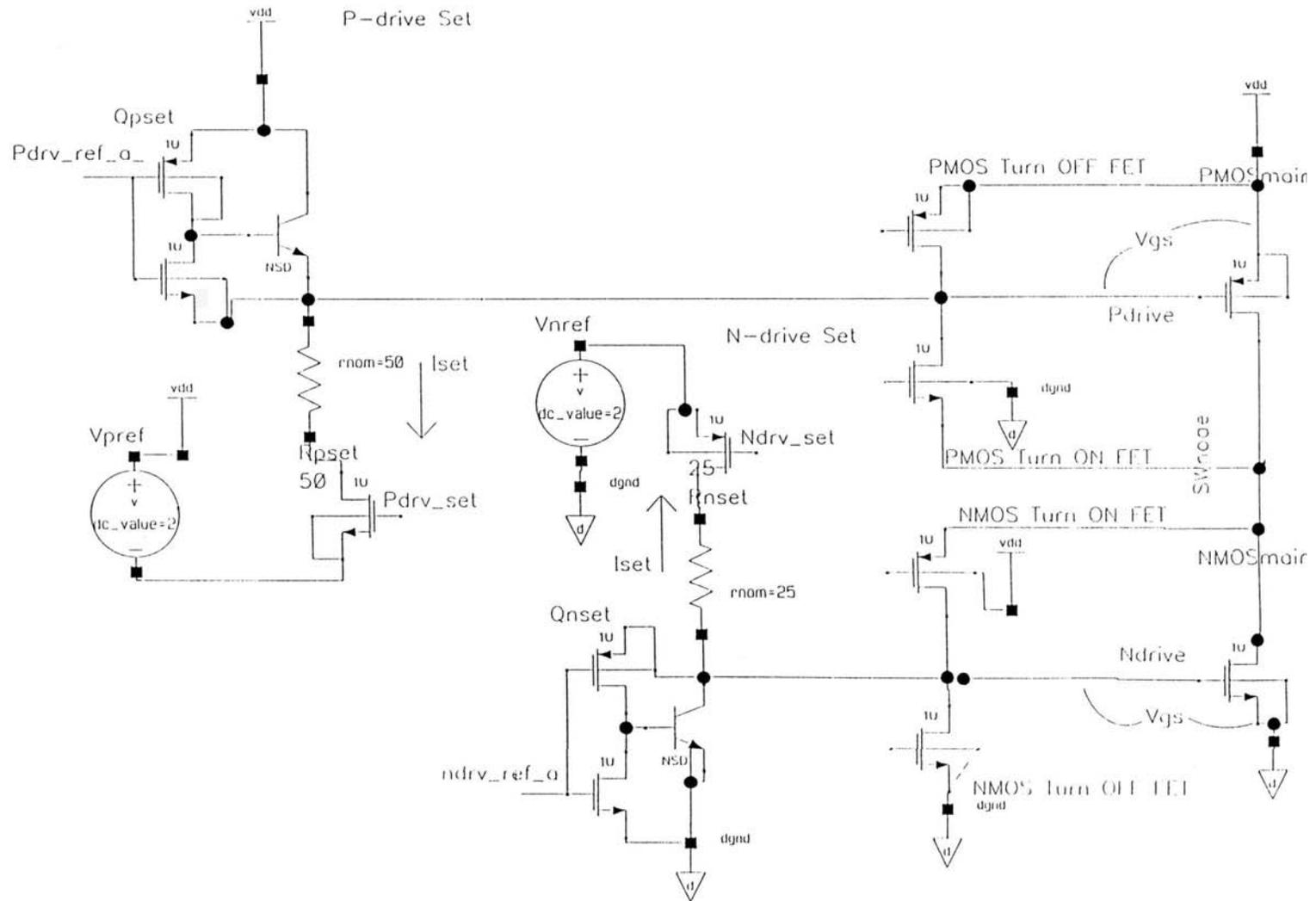


Figure 6-6 Diode drop with linear regulator gate voltage setting circuit.

### Gate voltage setting via FET clamping.

Instead of applying a reference voltage directly to the output MOSFET gates in setting  $V_{gs}$ , a higher impedance voltage reference can be applied directly to the gate of a clamping FET such as QPclamp shown in Figure 6-7. In the Figure, a  $V_{gs}$  setting mechanism is shown for the Pdrive; however, a similar approach equally applies to the Ndrive. As implemented above, a current source can be used to generate a voltage reference instead of a costly LDO, and still achieve reasonable accuracy. In the “FET clamping” approach, generally, a relatively small clamping FET is arranged in a source follower configuration whereby the reference voltage is applied to the gate of the clamping FET whose source monitors the output MOSFET’s gate, and acts to pull the output MOSFET’s gate voltage to within one  $V_T$  of  $V_{ref}$ . Referring again to Figure 6-7, to pull Pdrive  $V_{gs}$  towards full on, a small FET QPset is activated. When  $V_{ref}$  is set to the desired setting voltage the much larger QPclamp begins to turn on as  $V_{gs}$  approaches one  $V_T$  below  $V_{ref}$ , whereby QPclamp acts to oppose QPset and clamp  $V_{gs}$  to  $V_{set} = V_{ref} - V_T$ .

While QPclamp holds the Pdrive node at the  $V_{set}$  potential, a parallel sensing FET, Qsetkill, detects when the clamp turns on and sends a signal to terminate the setting process, whereby the output FET  $V_{gs}$  is left floating at the  $V_{set}$  potential. The  $RDS_{on}$  of QPset must be much less than that of QPclamp to minimize shoot-through current between QPclamp and QPset before QPsetKill terminates the  $V_{gs}$  setting process and for QPclamp to be strong enough to hold  $V_{gs}$  steady. This can force QPclamp to be quite large since its gate drive tends to be only one  $V_T$ , unlike QPset, which gets the full power



supply for gate drive. The setting accuracy depends on the variation in  $V_{ref}$  and the  $V_T$  of Qclamp. This could typically cause a 20-30% range in  $V_{set}$ .

### **Gate voltage setting via switch-node FET clamping**

The gate voltage setting approach presented herein is a variant of the FET clamping method described above. The difference is that instead of adding the FET QPclamp shown in Figure 6-7, the present design uses the existing gate drive FET Q\_ON\_SW as illustrated in Figure 6-8 operating in a dual use. As described in the energy-recycling chapter above, in the first stage of the  $V_{gs}$  setting process Q\_ON\_SW transfers energy from SWnode to the gate of the output FET to turn on. Once this FET is turned on the SWnode is guaranteed to have switched to the opposite supply potential than just before the transition. In this case, the symmetry of FET construction allows for the drain and source of Q\_ON\_SW to effectively reverse. In the 2<sup>nd</sup> stage, Q\_ON\_SW then acts to clamp  $V_{gs}$  to within one  $V_T$  of the gate voltage,  $V_{ref}$ , on Q\_ON\_SW, and uses the SWnode as a clamping power source. The draw back of this novel technique is that there is a reverse recovery time for Q\_ON\_SW that prevents it from clamping the  $V_{gs}$  immediately. This happens because the drain to source current  $I_{ds}$  of Q\_ON\_SW in stage 2 flows opposite to that of stage 1, and must reverse the FET's conduction channel charge distribution. This slower clamping time allows  $V_{gs}$  to overshoot  $V_{set}$  until Q\_ON\_SW recovers and begins clamping. This method applies to applications where the speed of the gate drive transition is slow enough to allow for a wait state until Q\_ON\_SW recovers and the  $V_{gs}$  setting process can begin. When this is not possible, then a stand-alone clamping FET, as QPclamp shown in Figure 6-7, is a preferred solution. Also as in the stand-alone clamping FET design, the  $RDS_{on}$  of QPset must be much less than that of

QPclamp . This can force Q\_ON\_SW to be quite large since its gate drive tends to be only one  $V_T$ , unlike QPset, which gets the full power supply for gate drive. However, given that Q\_ON\_SW is already sized relatively large so that it can turn on the large power FET PMOSmain, there is less penalty as compared to the stand-alone FET clamp.

### **Gate voltage setting via FET forcing**

The  $V_{set}$  forcing concept presented herein seeks to overcome the penalties of requiring a large QPset, losing energy when QPclamp fights QPset to hold the node at  $V_{set}$ , and large variations of QPset's  $R_{DSon}$  with  $V_{dd}$ . Figure 6-9 depicts one implementation of the  $V_{set}$  forcing method. It is very similar to the clamping scheme, except the N and P channel QPclamp FET's are exchanged with their complement polarities, and the clamp now becomes an active setting FET, or QPset. In the present design, QPset is configured in a source-follower arrangement, which has the effect of pulling as  $V_{gs}$  towards  $V_{set}$  until the gate drive bias of QPset gently tapers off as  $V_{ref} - V_{gs}$  goes below  $V_T$ . This mechanism, unlike the others, is largely independent of  $V_{dd}$ , and varies only with the process range of  $V_T$ ,  $I_{set}$ , and  $R_{set}$ . Moreover, the size of QPset is much smaller because it gets a larger gate drive, and only needs to supply a very small current to lift the main output FET's after they are turned on. It should be noted that  $V_T$  should be as small as possible since it limits the minimum  $V_{dd}$  the circuit can operate at, according to  $V_{ref} = V_{set} + V_T$ . As will be shown below, another major benefit of the forcing method is that QPset can also be used to help turn on the output FET during normal, full  $V_{gs}$  operating mode.



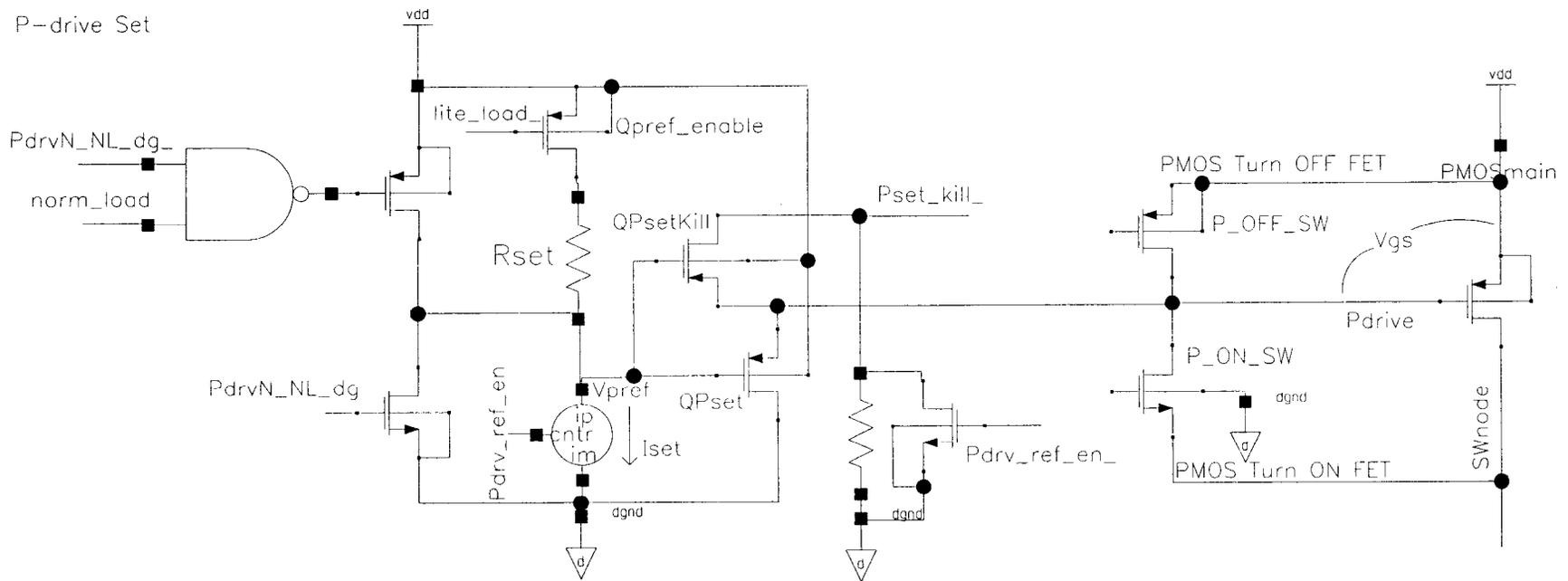


Figure 6-9 Gate voltage setting circuit using FET forcing.

The graph in Figure 6-10 illustrates the  $V_{gs}$  setting results for N-drive, wherein  $V_{set}$  is targeted to a 2.1V  $V_{gs}$  that transitions within 30ns, over a supply range of 3.6 to 5.5V. All device parameters are held constant over  $V_{dd}$ . As can be seen, the energy recycling gate-drive mechanism drives N-drive over the 1V  $V_T$  required to turn on NMOSmain within 5ns. The slower  $V_{gs}$  setting process by way of FET forcing begins at about 3.125us and within about 25ns  $V_{gs}$  is gradually raised to the target set point of about 2V. A 5% setting error is observed. It should be understood that a similar approach applies equally to the P-drive  $V_{gs}$  setting process.

### **Conclusion**

Several gate drive methods of limiting the  $V_{gs}$  of push-pull configured MOSFETs have been presented. Each method initially turns on the output MOSFET with recycled energy as prescribed by the present Thesis. After turn-on, various low energy  $V_{gs}$  setting mechanisms drive the voltage to the target value. Each method has certain advantages and disadvantages that the system designer can select to optimally match the constraints of the particular application, thereby improving operational robustness.

The presented methods add negligible incremental cost or complexity, while significantly reducing the amount energy used to switch on and off push-pull configured MOSFETs, thereby significantly increasing power efficiency, especially under light-loading conditions.

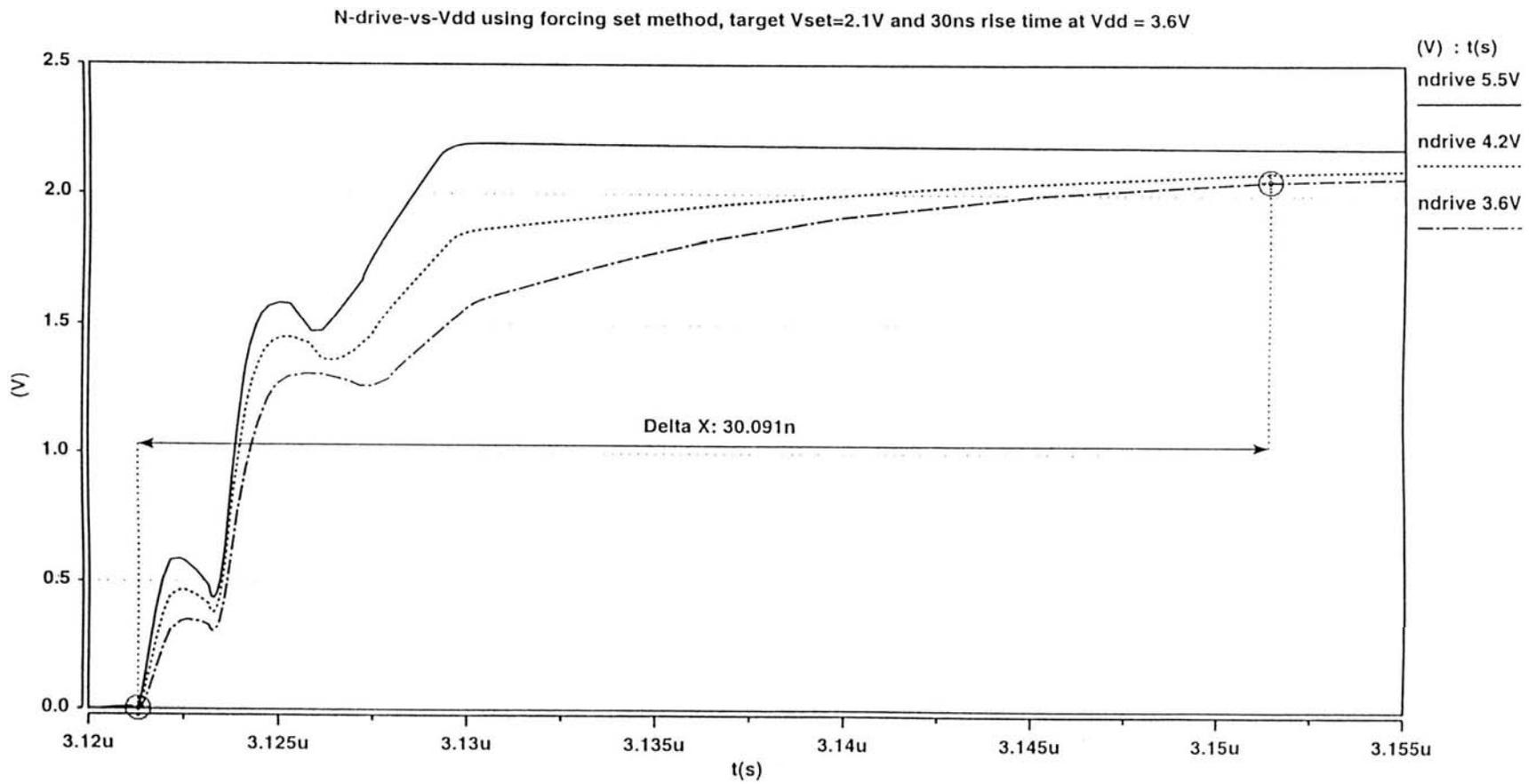


Figure 6-10 FET forcing method family of curves for  $V_{dd}$  ranging from 3.6V to 5.5V.

## CHAPTER 7 SYNCHRONOUS BUCK SYSTEM IMPLEMENTATION AND RESULTS

### **System Implementation**

The synchronous buck regulator design presented herein is generally derived from a standard buck topology with modified gate drive and light-load detection systems. The novel contribution is in the way the gate drive turns on the main output FET's. The known architecture has one very large gate drive FET that pulls energy from the supply to the gate of output FET, independent of loading. The proposed technique has a two-fold approach. One is to take energy from the switch-node to turn on the output FET's, and then to use that node to also time the start of a gate drive  $V_{gs}$  setting procedure. On the system level, it is important that the gate drive transition occurs within a certain period of time to guarantee a minimum duty cycle operation at the highest  $V_{dd}$  and for the largest output FETs specified. The circuits described are best applied to integrate circuit technology, but equally apply to discrete designs. Furthermore, it is important that there be maximum flexibility to the designer to adjust all parameters to meet the specifications of a given application. The design must also be very robust, and have typical failure modes that still permit useful, but possibly less efficient, operation. One embodiment that achieves this goal is instantiated in the schematic shown in Figure 7-1. In the Figure, only the P-drive circuitry is shown and other well known details have been omitted for clarity. The N-drive circuitry is similar to the P-drive with polarities complimented. The FET forcing, low  $V_{gs}$  setting method described in Figure 6-9 is implemented and, although not shown, the light-load detection system illustrated in Figure 5-1 is used to

generate the normal load (norm\_load) signal applied to the NAND gate in Figure 6-9.

Hence, the discontinuous mode is used to detect the light-load condition. This is sensed at the switch-node (SWbuckint) by a positive-going signal, which indicates that the  $L_{\text{buck}}$  inductor (**ind**) is out of energy and charging in the reverse direction. This crossover point is load dependent and occurs when the average output ( $I_o$ ) current minus switching current ( $I_{\text{ind}}$ ) goes negative, or *light\_load* is when  $I_o - .5 * I_{\text{ind}}$  is  $< 0$ . Thus, a desired *light\_load* trigger point can be reliably designed for by choosing the value of  $L_{\text{buck}}$  to provide a certain maximum load-current trip point over the full range of  $V_{\text{dd}}$ . The selection of  $L_{\text{buck}}$  is well known, and can be found by way of the inductor equation  $V = L di/dt$ . The trip point is usually not very critical as long as the worst-case situation meets specifications. When in *light\_load* mode the  $V_{\text{gs}}$  of the output FETs is limited to a voltage set by the  $V_{\text{gs}}$  setting block.

Referring again to Figure 7-1, in the first phase of the  $V_{\text{gs}}$  setting process the switch-node connected FET QPonSW turns on the output FET PMOSmain. However, to improve robustness in the case where there may not be enough recycled energy to turn-on PMOSmain fast enough, there is a *light\_load* FET (QPonLL) that supplies energy from the power supply. QdrvLL is intended to be small (about 24 ohms in this design) and is mainly to improve robustness. Transistor QPonSW should be chosen large enough (1.3 ohms in this design) to turn-on PMOSmain in the worst case. In the second phase of the  $V_{\text{gs}}$  setting process, a FET called Pset forces  $V_{\text{gs}}$  of PMOSmain to the desired  $V_{\text{set}}$  gate-drive voltage value. Once set, the gate of PMOSmain is left floating, and fully on, until the PWM controller turns PMOSmain off a manner similar to prior-art.

In the *normal\_load* mode, *Qon\_SW*, again, ensures the output FET's are turned on. There is a FET called *QdrvNL* that activates in parallel with *Qon\_SW* to guarantee  $V_{gs}$  will transition across the full supply voltage range, within some specified maximum time. *QdrvNL* should be small, and is meant to fully swing the node beyond where *Qon\_SW* turns off. To fully employ all assets, the FET's *QdrvLL*, *QdrvNL*, *Qon\_SW*, and *Pset* all turn on simultaneously. This means that in integrated circuit implementations, the die area that would have been used to meet a certain turn on specification for the output FET in a standard, prior-art, design, should equal the total area of these FET's in the present system. In our example, the worst-case rise time was targeted for 5.5V in 30ns.

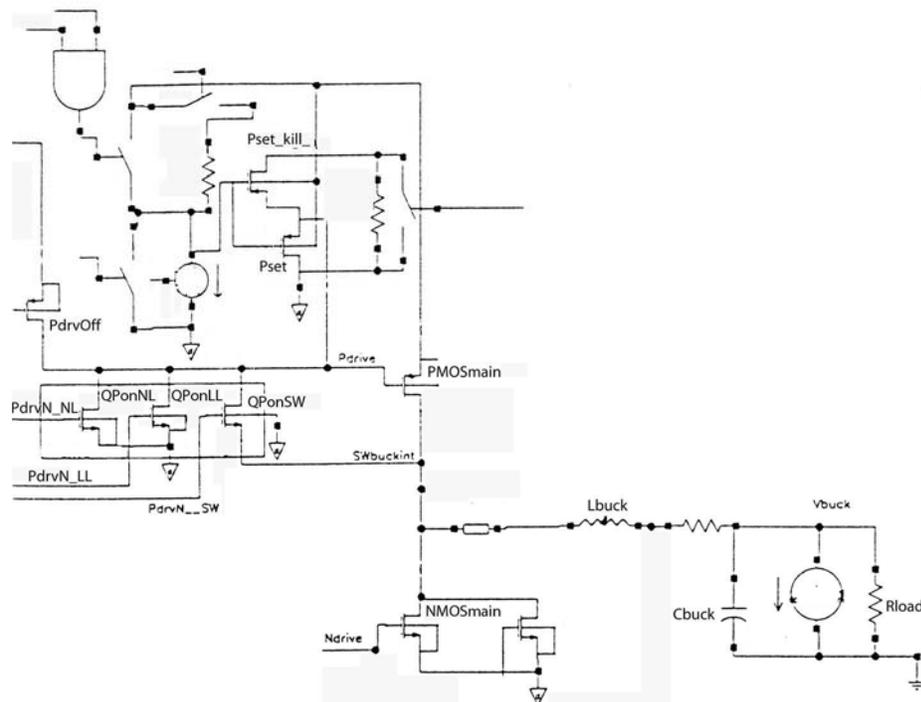


Figure 7-1 Synchronous buck P-drive implementation.

P-drive control signal timing in both light and normal load modes (Vdd=3.6V, I<sub>L</sub>= 1ma to .75A)

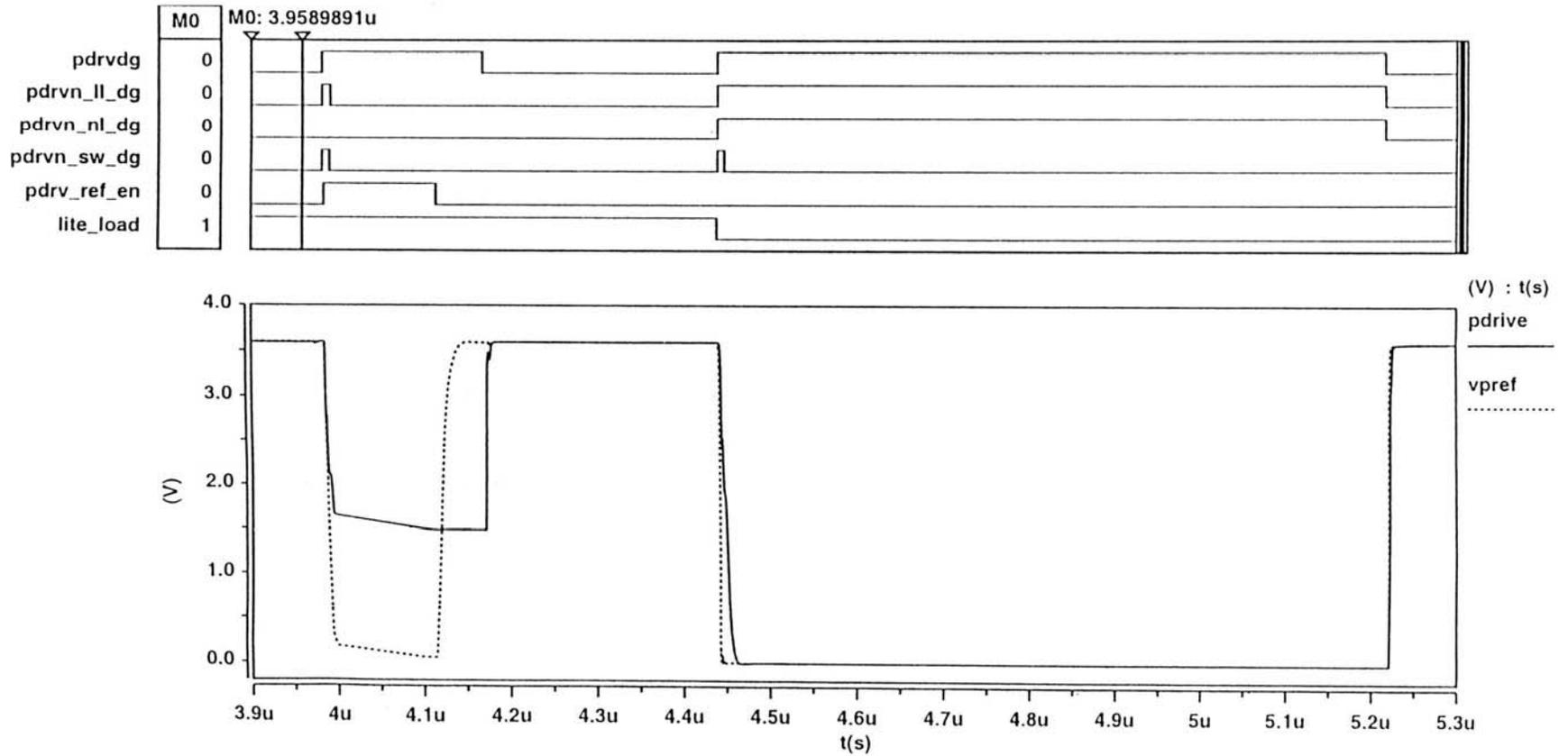


Figure 7-2 P-drive signal timing diagram under light and normal loading conditions.

Figure 7-2 and Figure 7-3 illustrate signal timing diagrams of how the gate drive control signals behave in both *light\_load* and *normal\_load* conditions for the P-drive and N-drive respectively. The top group of signals is digital, and the lower group analog. Referring initially to Figure 7-2, the signals *pdrv* and *ndrv* are digital representations of the analog P-drive and N-drive, respectively. The digital signals *pdrvn\_ll\_dg*, *pdrvn\_nl\_dg*, and *pdrvn\_sw\_dg* are the control signals that activate, respectively, the light-load assist FET QPonLL, the normal load assist FET QPonNL, and the switch-node energy recycling FET QPonSW. The digital signal *pdrv\_ref\_en* turns-on the  $V_{ref}$  reference voltage. The digital signal *light\_load* is active high during light-loading conditions and zero otherwise. In the analog signal group, the *pdrive* signal is the voltage at the gate of PMOSmain, and the signal *vpref* is the reference voltage  $V_{ref}$  used to set  $V_{gs}$  of PMOSmain to the desired  $V_{set}$  gate drive voltage value during the second phase of the  $V_{gs}$  setting process. The signals in Figure 7-3 follow the same nomenclature pattern as described for Figure 7-2 except that “p” is replaced with “n”; e.g., “vpref” becomes “vnref.”

In the Figures, it is seen that the light-load assisting FETs turn on only during the first phase when the output FETs are initially turned on with  $V_{gs}$  clamped to just above  $V_T$ . This ensures a robust turn on. Thereafter, the reference voltage  $V_{ref}$  is enabled and the  $V_{gs}$  gate voltage is gradually brought to its final  $V_{set}$  set point, and thereby fully turned on. In normal load operating mode, it is seen that  $V_{gs}$  is driven across the fully supply voltage swing as in prior-art designs, thereby minimizing the output FET’s conduction resistance  $R_{dsON}$ , which is the dominant power loss factor above light-loads.

N-drive control signal timing in both light and normal load modes (Vdd=3.6V, I<sub>L</sub>= 1ma to .75A)

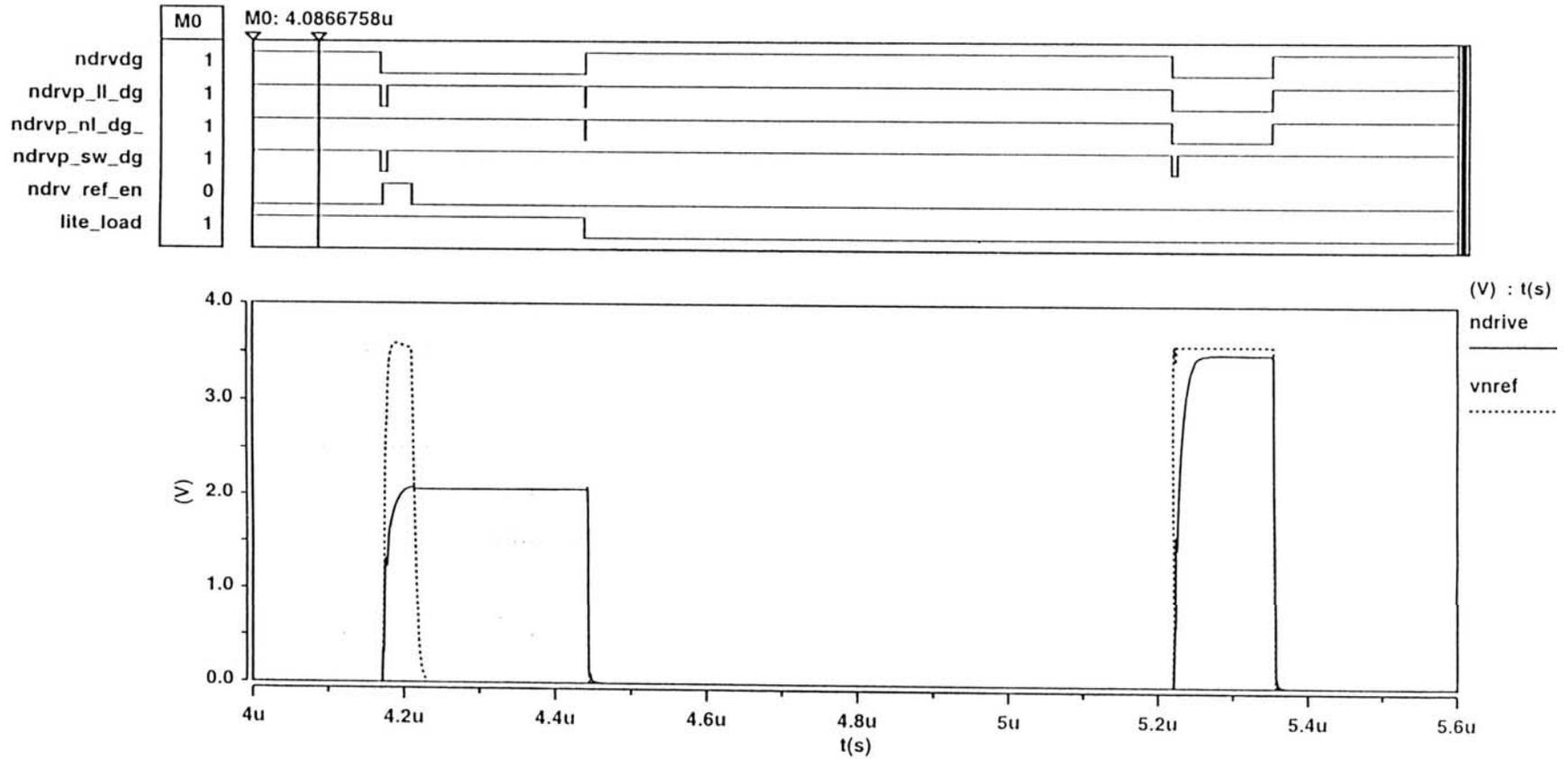


Figure 7-3 N-drive signal timing diagram under light and normal loading conditions.

## Efficiency Results

### Efficiency Benefit at Normal Loads

The benefits of increased switching efficiency to the overall power efficiency of a buck regulator depends on loading current  $I$  as was shown in Equation (1). The FET's conduction resistance ( $R_{dsON}$ ) dominates the power loss equation beyond light-load operating currents. Although the present design does not significantly increase buck power efficiency outside light-loading conditions, or at normal loads, the energy recycling FET connected to the switch-node still provides most of the turn on energy. Figure 7-4 graphs the current contribution of each turn-on FET to turning the NMOSmain output FET on in normal load mode. As seen in the Figure, the recycled drive current provided by QNonSW, labeled as  $ids\_Ndrive\_SW$ , is about twice that provided by the power supply derived current ( $ndrvp\_nl/ids$ ). In prior-art designs, this recycled energy is wasted. Up to a certain limit, the gate drive receives more "free" energy from the switch-node SWbuckint as the size of QNonSW is increased. However, at normal loads the observed benefit to efficiency is only a few percent. The foregoing discussion directed to the N-drive signals shown in Figure 7-4 similarly applies to the P-drive as well.

### Efficiency Benefit at Light-loads

At light-loads, it can be seen that for practical values used in Equation (1), increased switching efficiency can significantly increase the overall power efficiency of a buck regulator, and is largely unaffected by loading current  $I$ . That is, the switching frequency  $f_s$  term dominates over  $R_{dsON}$  in Equation (1). The squared  $V_{gs}$  factor of the  $f_s$  term is a particularly high penalty reducing efficiency as  $V_{gs}$  is increased.

N-drive control signal timing in both light and normal load modes (V<sub>dd</sub>=3.6V, I<sub>L</sub>= 1ma to .75A)

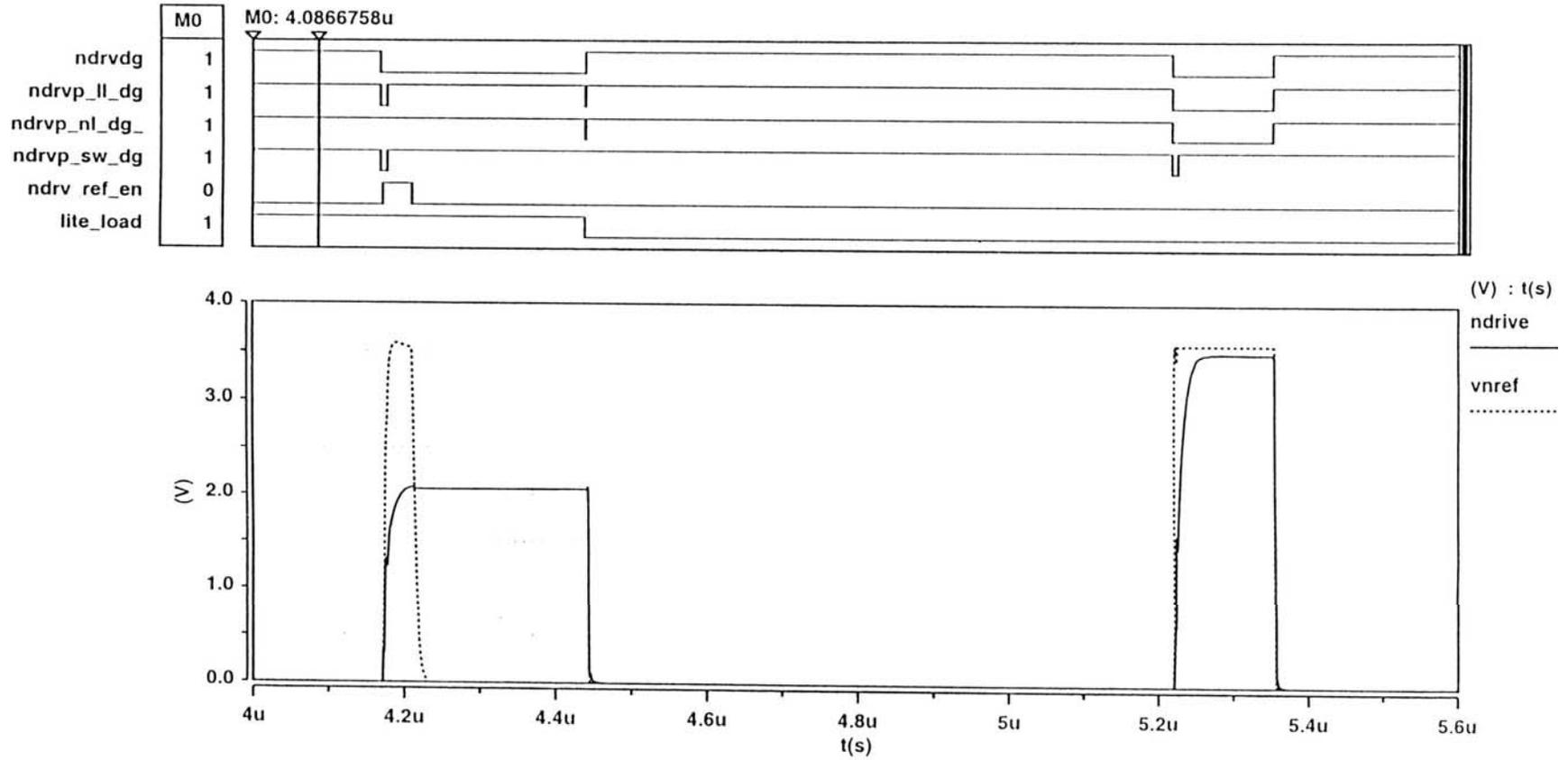


Figure 7-4 Low V<sub>gs</sub> normal load gate drive currents at N-drive turn-on.

Referring briefly back to Figure 7-1, it should be understood that the prior-art and low  $V_{gs}$  results herein presented are intended to be directly comparable and therefore are based on designs that use the same output power MOSFETs, inductor  $L_{buck}$ , and capacitor  $C_{buck}$ . Furthermore, for both results the operating frequency is set at 250KHz, supply voltage ( $V_{batt}$ ) at 10V, output voltage ( $V_{buck}$ ) of 1.8V, and a load-current of 250mA. The power MOSFETs used for PMOSmain is the Fairchild FDC6312CP, and Fairchild FDG327N for NMOSmain. The FDG327N is a 1.5A, 1.8V NMOS FET that has a  $V_T = .7V$  (typ.),  $C_g = 420pF$ ,  $R_{dsON} = 140$  mOhm @1.8V, and output capacitance of 87pF. The FDC6312CP is a 2A, 1.8V PMOS FET that has a  $V_T = -.9V$  (typ.),  $C_g = 467pF$ ,  $R_{dsON} = 225$  mOhm @-1.8V, and output capacitance of 85pF. The parasitic capacitance of these FETs is closely matched, which provides a similar amount of recycled turn-on energy for each FET in the present low  $V_{gs}$  design.

Figure 7-5 and Figure 7-6 illustrate a simulation of switching signals over two cycles for the prior-art and present low  $V_{gs}$  designs, respectively. It is clearly seen that the full supply voltage swing of Pdrive and Ndrive in the prior-art design induces significantly larger voltage spikes at the switch-node ( $SW_{buck}$ ) than that of the present low  $V_{gs}$  design. The higher switching currents of the prior-art design similarly causes greater noise in the power supply, especially in battery supplied systems. Prior-art noise spikes are about 4 Vs above and below ground, whereas the present low  $V_{gs}$  design has only about 0.5 V. In Figure 7-6, the low  $V_{gs}$  set points are approximately 2.5V for Ndrive, and 2.2V for Pdrive.

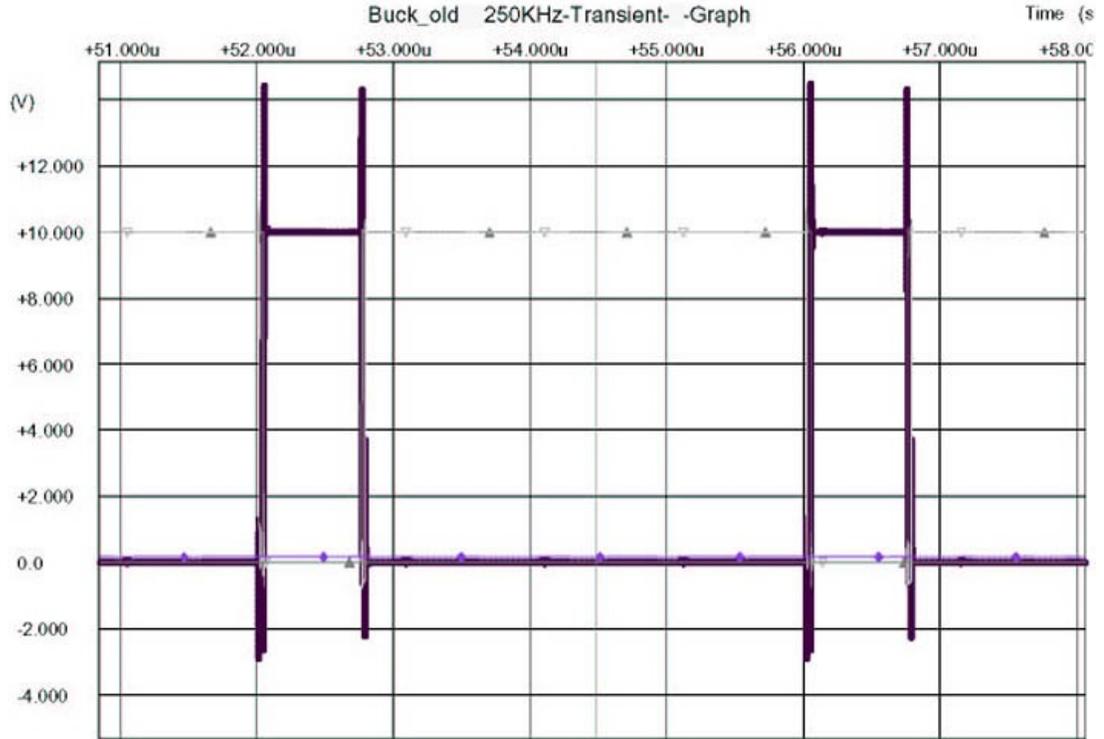


Figure 7-5 Prior-art switching signals at light-load.

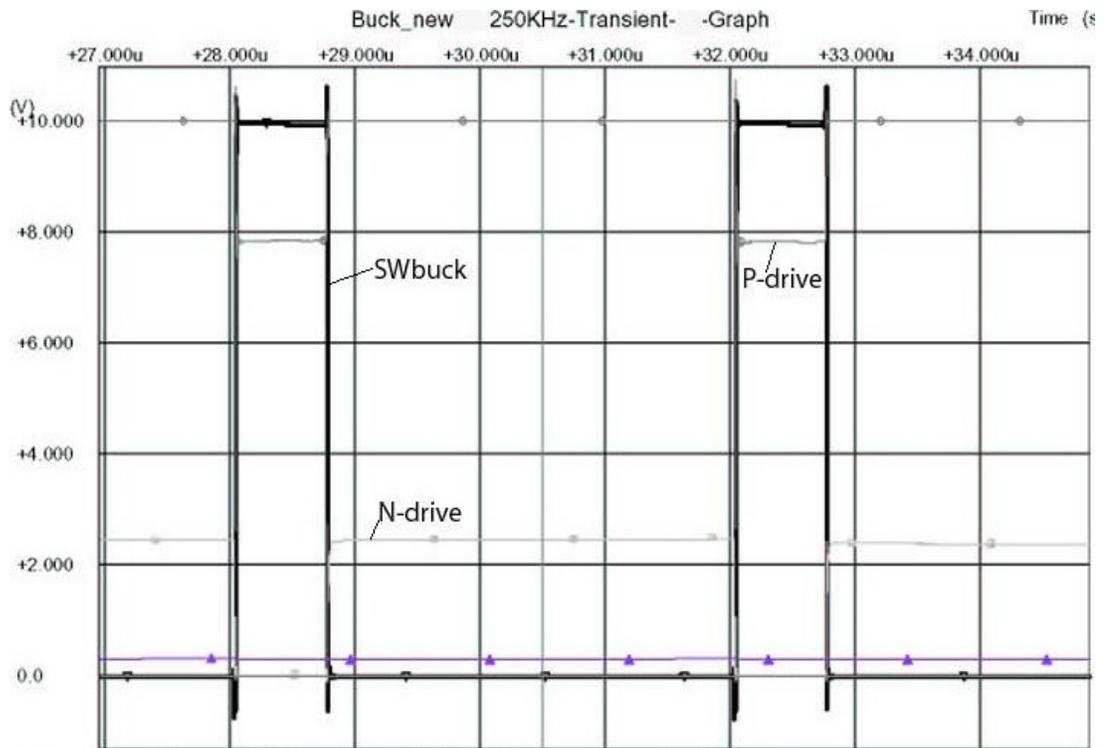


Figure 7-6 Low  $V_{gs}$  switching signals at light-load.

Figure 7-7 and Figure 7-8 illustrate simulation results at the point when SWbuck is turned on in the prior-art, and present low  $V_{gs}$  designs, respectively. It is clearly seen that the switching currents in the prior-art approach are significantly greater the present low  $V_{gs}$  method. To turn off the NMOS (N-drive off) over 10A of power supply current ( $I_{batt}$ ) is required verses only 0.5A in the low  $V_{gs}$  design. Similarly, to turn on the PMOS (P-drive on) takes prior-art over 8.5A, and low  $V_{gs}$  only 6A. In Figure 7-8, P-drive turns on within 3 ns and reaches its terminal set point of about 2.1V in about 7ns, which is sufficiently fast to support high frequency operation above 1.5 MHz, and to keep transient power losses in the PMOS FET to a minimum.

Figure 7-9 and Figure 7-10 show similar simulation results at the point when SWbuck is turned off in the prior-art, and present low  $V_{gs}$  designs, respectively. To turn off the PMOS (P-drive off) takes over 9A from  $I_{batt}$  in the prior-art design verses only about 4A in the low  $V_{gs}$  case. Similarly, to turn on the NMOS (N-drive on) takes prior-art over 5.5A, whereas the low  $V_{gs}$  approach only requires just over 2A. In Figure 7-10, N-drive turns on within 5ns and reaches its terminal set point of about 2V in about 25n, which is more than sufficient to support high frequency operation, and to keep transient power losses in the NMOS FET to a minimum.

The present low  $V_{gs}$  approach results in a significant increase in power efficiency due to the associated lower switching currents. In the foregoing example, the low  $V_{gs}$  buck regulator achieves about 30% efficiency, which was twice as much as the prior-art system of about 15%. The equation used to calculate power efficiency  $\eta$  is given by the following Equation: (2):

$$\eta = \frac{V_{buckRMS} * I_{buckRMS}}{V_{battRMS} * I_{battRMS}} * 100 \quad (2)$$

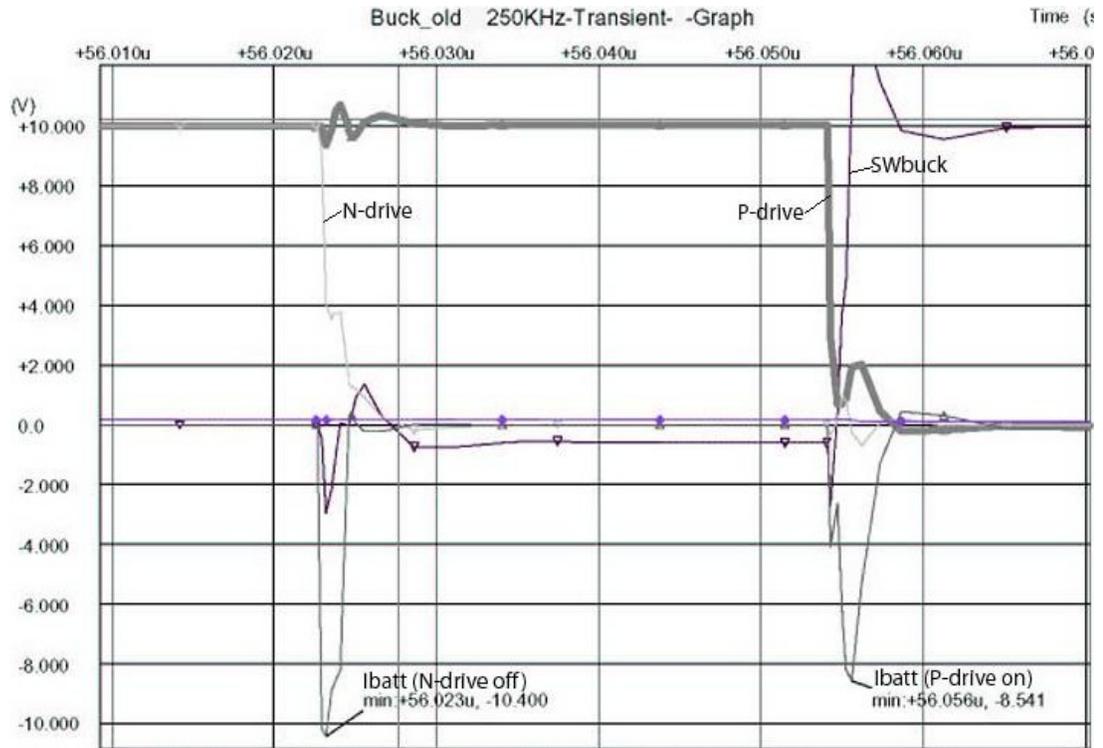


Figure 7-7 Prior-art light-load gate drive signals at switch-node turn on.

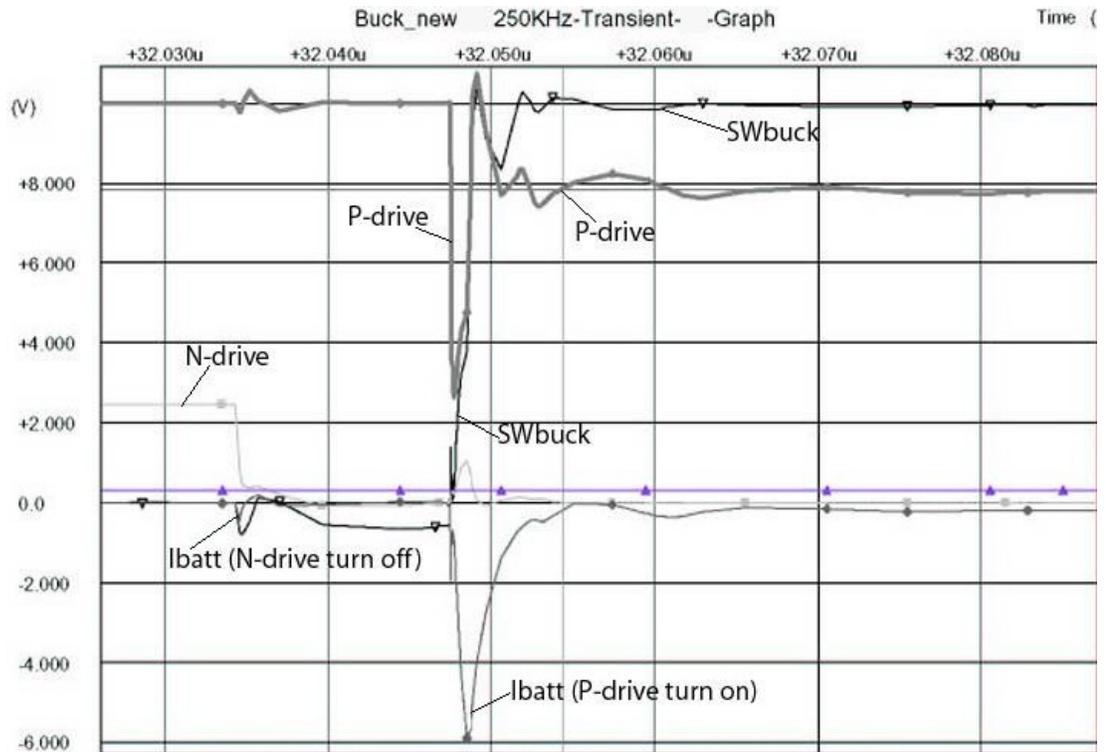


Figure 7-8 Low  $V_{gs}$  light-load gate drive signals at switch-node turn on.

As a reference, if a linear regulator was outputting 1.8V, efficiency would be about 18% (1.8/10). Strictly from an efficiency point of view, applications having an input voltage that is significantly higher than the output regulation voltage should implement a switching regulator. The regulator that generated the foregoing simulation results is capable of about 2A continuous, operating at an efficiency above 90%. At higher switching frequencies, efficiency for significantly decreases at light-loads. For example, in the above design, if the switching frequency is increased to 1 MHz and load-current decreased to 100 mA, efficiency drops to as low as 0.35% in the prior-art design. The present low  $V_{gs}$  method still provides a significant efficiency benefit at around 12%.

If instead, voltage is decrease, and load-current is held constant, overall efficiency improves and the benefit of the present methods decreases, but is still significant. By way of example, if  $V_{batt}$  is decreased from 10V to 6V at 250 mA, efficiency is about 35% in the prior-art approach, and 50% for the low  $V_{gs}$  design. Thus, the system designer implementing the present low  $V_{gs}$  method will determine the  $C_g$  range to be supported and design the light-load detection system to activate at the optimal combination of  $V_{batt}$ ,  $V_{buck}$ , and  $I_{load}$ .

### Conclusion

A novel buck switching regulator design has been presented that efficiently switches on and off relatively large power MOSFET configured in a push-pull binary arrangement. At relatively high supply voltages, switching currents have been demonstrated to be less than half that of a known standard approach. Generally, as switching losses increasingly dominate in the synchronous buck regulator efficiency, the present low  $V_{gs}$  method will provide increasing benefit. In battery operated applications that have relatively high battery voltages and/or high switching frequencies operating at

light-loads for long periods, the present approach can significantly decrease overall power consumption, thereby increasing battery life. Importantly, the presented light-load efficiency benefits of the present design come at little incremental cost, and minimal increase in system complexity. Generally, buck regulators capable of over 0.5A operating at switching frequencies above 250KHz, input voltages above 5V, and load-currents below 250 mA will receive significantly higher light-load efficiency than otherwise possible with the currently available state-of-the art. Moreover, given that many modern MOSFETs are designed to be fully turned on at 2.5 V, or less, the present method can even provide benefits at normal load-currents by way of significantly lower noise induced into the system due to the much smaller switching currents. Switching regulator noise is a significant, and sometimes crippling, problem in RF and analog sensor systems.

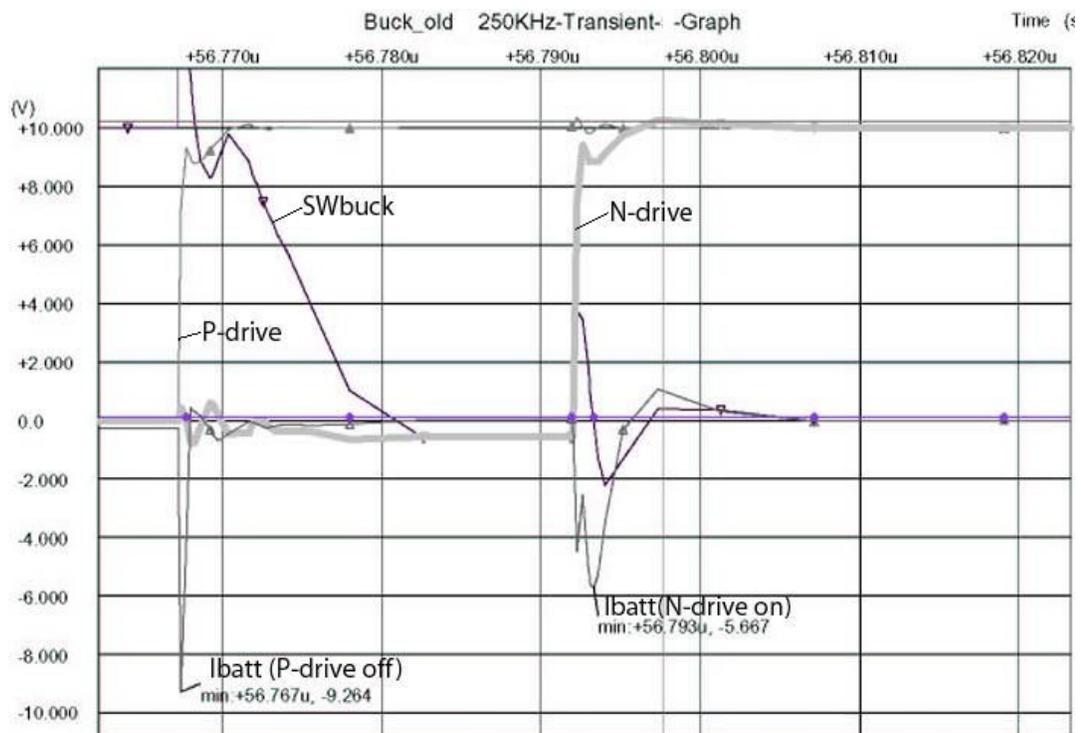


Figure 7-9 Prior-art light-load gate drive signals at switch-node turn off.

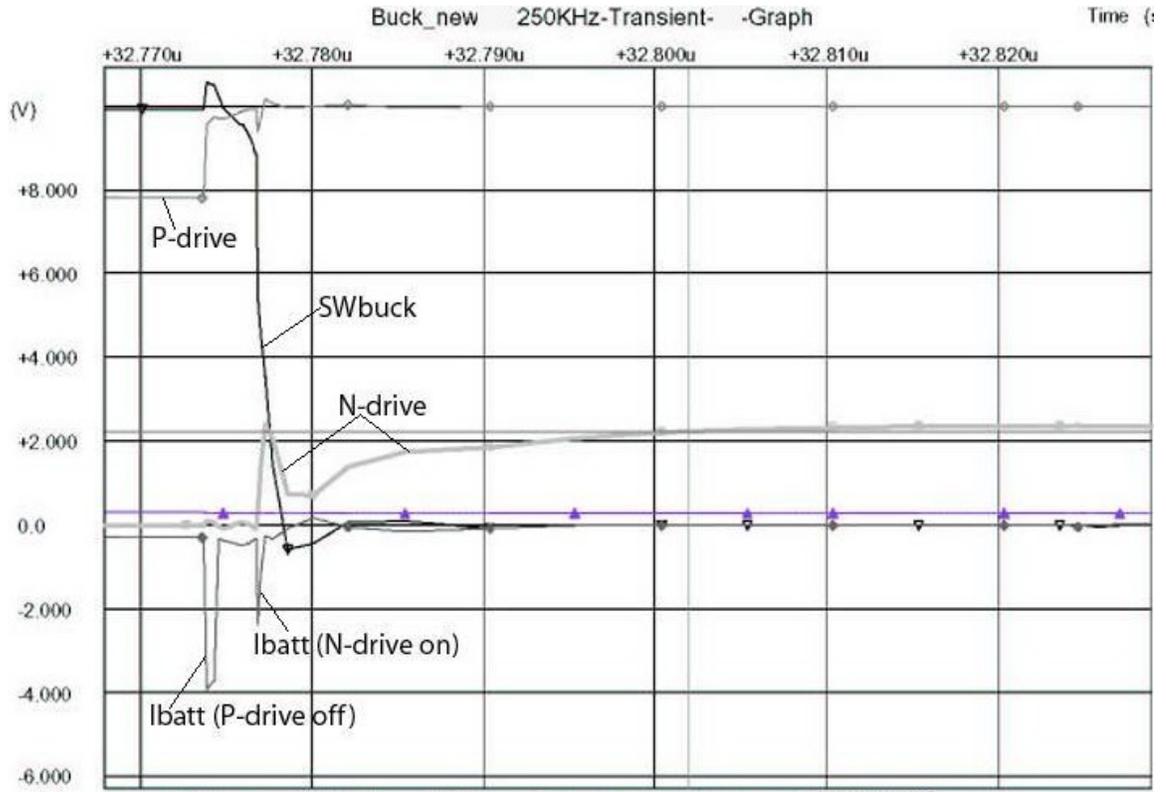


Figure 7-10 Low  $V_{gs}$  light-load gate drive signals at switch-node turn off.

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## BIOGRAPHICAL SKETCH

Mr. BenTolila earned a B.S. in Electrical and Computer Engineering from the University of Florida where he graduated with High Honors in the top 10% of his class and was on the Dean's Honor List, and twice received the President's Outstanding Student Award. He continued at University of Florida for his Master's work in Robotics.

His areas of specialty include algorithms, advanced modeling/simulation, artificial intelligence, pattern recognition, data mining, mobile robotics, sensors, analog/digital systems, power management, software, embedded real-time applications, signal processing, battery technology, and wireless systems. He possesses a particular in-depth knowledge of switching regulator systems, robotic systems, and machine learning methods such as fuzzy logic, neural networks, hidden markov models, and genetic algorithms. Beyond technology, Mr. BenTolila has significant experience in business models, and finance.

Mr. BenTolila has enjoyed a wide variety of industry experience. His most recent post was as Patent Engineer at a Silicon Valley intellectual property (IP) law firm. Prior employment in Silicon Valley includes Software Marketing and Corporate IP Manager for a pre-IPO start up in embedded speech recognition solutions. Prior to this position, he gained important Research and Development experience at a pre-IPO start up in Interactive TV advertising as an Artificial Intelligence Research Scientist, where in addition to many other co-inventions, he was the sole inventor in three key patents pending covering machine learning, data mining, intelligent agents, and user preference

modeling. Earlier, Mr. BenTolila gained solid technical expertise in mixed-signal semiconductor products as a Systems Research Engineer at a Fortune 500 semiconductor company. He worked on cell-phone power management systems, behavioral simulation methodologies, Li-Ion battery modeling, and switching regulator designs. Other past positions include Research Electronics Engineer at Southwest Research Institute (SRI) and the National Institute of Standards and Technology (NIST). At SRI, he worked in the Automation and Data Systems Division, where Mr. Bentolila was the lead designer of a fuzzy logic tactile robotic arm controller, and engaged in applied sensor fusion research. At NIST, he was under the Intelligent Systems Division, Robot Systems Integration Group. Among many other mobile robot endeavors, Mr. Bentolila developed sensors and systems that enable bomb disposal, mobile robots to convoy.